FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13602-3E

16-bit Proprietary Microcontroller

CMOS

F²MC-16L MB90670/675 Series

MB90671/672/673/T673/P673 (MB90670 Series)
MB90676/677/678/T678/P678 (MB90675 Series)

■ DESCRIPTION

The MB90670/675 series have been developed as a general-purpose version of the F²MC*1-16L family consisting of proprietary 16-bit, single-chip microcontrollers. These general-purpose devices are designed for applications that require high-speed real-time processing suitable for process control in a wide variety of industrial and OA equipment.

The instruction set is based on the AT architecture of the F²MC-8 family, with additional high-level language supporting instruction, expanded addressing modes, enhanced multiplication and division instructions, and improved bit processing instructions. In addition, long-word data can now be processed due to the inclusion of a 32-bit accumulator.

The MB90670/675 series includes a variety of peripherals on chip, such as a UART, an SCI, a 10-bit A/D converter, an 8-bit PPG, a 16-bit reload timer, a 24-bit free-run timer, an OCU, an ICU, DTP/external interrupts, and I²C interface*2 (675 series only). Furthermore, because the on-chip peripherals, with the aid of intelligent I/O service function, can transfer data without the intervention of the CPU. This microcontroller can be used for applications that require real-time control.

*1: F²MC stands for FUJITSU Flexible Microcontroller.

*2: Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

■ FEATURES

- Minimum execution time: 62.5 ns at 4 MHz oscillation (with multiply-by-4 setting)
  PLL clock multiplier system used
- Instruction set optimized for controller applications
  Variety of data types: bit, byte, word, long-word
  Expanded addressing modes: 23 types
  High coding efficiency
  Improvement of high-precision arithmetic operations through use of 32-bit accumulator
- Instruction set supports high-level language (C language) and multitasking
  Inclusion of system stack pointer
  Variety of pointers
  High instruction set symmetry
  Barrel shift instruction

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MB90670/675 Series

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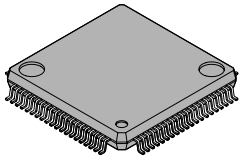
- Improved execution speed: 4-byte queue
- Powerful interrupt functions
  Priority levels: 8 levels (programmable)
  External interrupt inputs: 4 channels
- Automatic transfer function independent of CPU
  Intelligent I/O Service: max.10 channels
- General-purpose ports: max.65 channels (MB90670 series)
  max.84 channels (MB90675 series)
- 18-bit timebase counter
- Watchdog timer
- UART0: 1 channel
  Can be used for either asynchronous transfer or synchronous transfer
- UART1 (SCI): 1 channel
  Can be used for either asynchronous transfer or serial transfer with clock (I/O extended serial)
- A/D converter: analog inputs: 8 channels
  Resolution: 10 bits (switchable to 8 bits)
  RC-type sequential comparison method
- 24-bit free-run timer: 1 channel
- ICU (input capture): 4 channels
- OCU (output compare): 8 channels
- 8-bit PPG timer: 2 channels
- 16-bit reload timer: 2 channels
- I^2C* interface: 1 channel (only in the MB90675 series)
- Low-power consumption modes
  Sleep mode
  Stop mode
  CPU intermittent operation mode
  Pseudo-watch mode
  Hardware standby pin
- Packages: LQFP-80, QFP-80, LQFP-100, QFP-100
- CMOS technology
- I^2C License
  Purchase of I^2C components convey the Philips I^2C Patent Rights to use these component in an I^2C system, provided that the system comforms to the I^2C standard specification as defined by Philips.

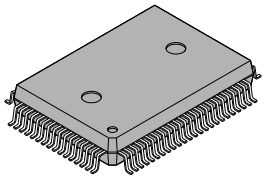
■ PACKAGE

80-pin Plastic LQFP



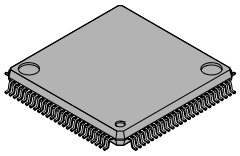
(FPT-80P-M05)

80-pin Plastic QFP



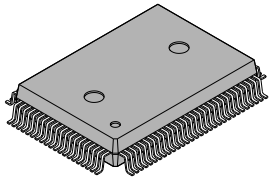
(FPT-80P-M06)

100-pin Plastic LQFP



(FPT-100P-M05)

100-pin Plastic QFP



(FPT-100P-M06)

MB90670/675 Series

■ PRODUCT LINEUP

- **MB90670 Series**

Parameter \ Part number		MB90671	MB90672	MB90673	MB90T673	MB90P673
Classification		Mass production products				One-time PROM product
CPU core	Number of instructions	340				
	Minimum execution time	62.5 ns at 4 MHz (PLL: with multiply-by-4 setting)				
	RAM size	640 bytes	1.64 Kbytes	2 Kbytes		
	ROM size	16 Kbytes (internal mask ROM)	32 Kbytes (internal mask ROM)	48 Kbytes (internal mask ROM)	None	48 Kbytes (internal OTPROM)
	System clock oscillation circuit	System clock/PLL clock on chip				
	Low-power consumption modes	Sleep, stop, CPU intermittent operation, pseudo-watch, hardware standby				
	Interrupts	Interrupt sources: 19 channels; priority levels: 8 (programmable); external interrupt inputs: 4 channels				
Resources	Ports	Output ports (N-channel open drain): 8 I/O ports (CMOS): 57 Total: 65				
	UART0	8 bits × 1 channel				
	UART1 (SCI)	8 bits × 1 channel				
	A/D converter	10-bit resolution × 8 channels				
	24-bit free-run timer	24 bits × 1 channel				
	ICU (input capture)	24 bits × 4 channels				
	OCU (output compare)	24 bits × 8 channels				
	8-bit PPG timer	8 bits × 2 channels				
	16-bit reload timer	16 bits × 2 channels				
	I^2C interface	None				
	Watchdog timer function	On chip				
Characteristics	Power supply voltage	+2.7 V to +5.5 V				
	Operating temperature	–40°C to +85°C				
	System clock frequency	32 MHz (+5.0 V ± 10%) 16 MHz (+3.0 V ± 10%)				
Miscellaneous	Package	FPT-80P-M05/FPT-80P-M06				
	Process	CMOS				

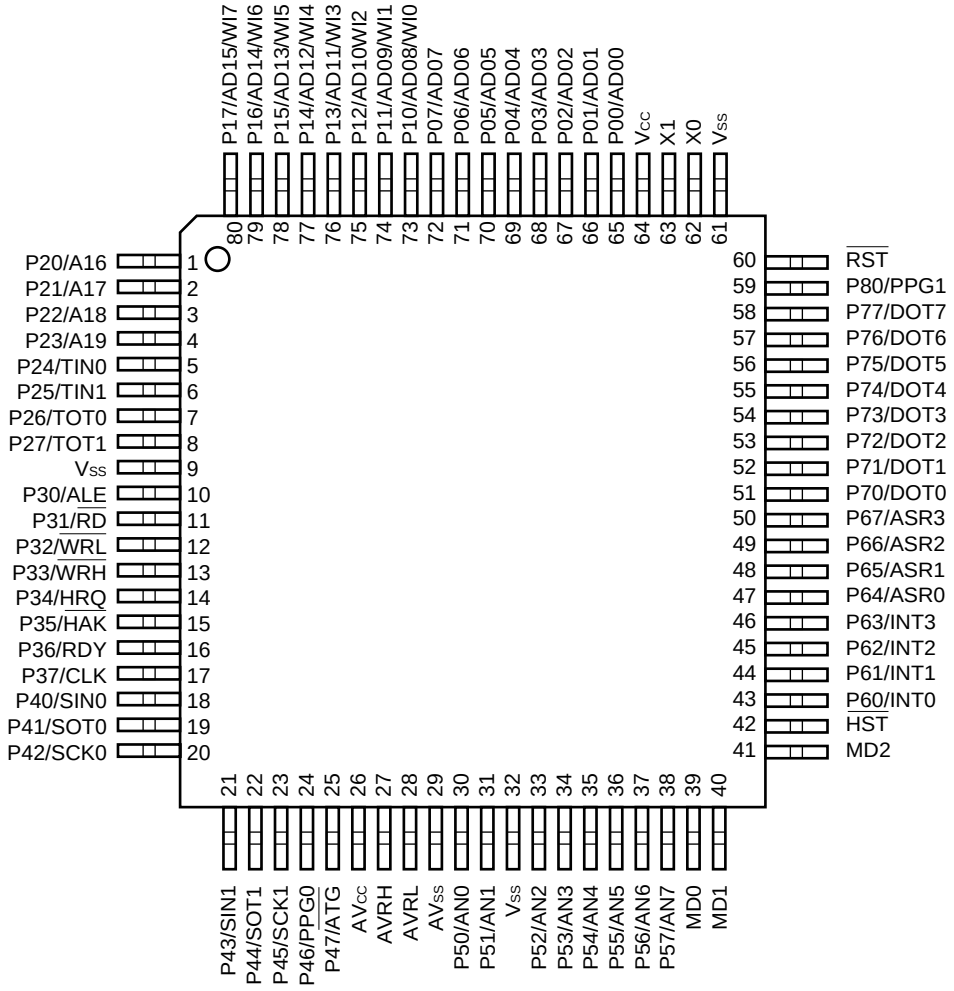
- **MB90675 Series**

Parameter \ Part number		MB90676	MB90677	MB90678	MB90T678	MB90P678
Classification		Mass production products				One-time PROM product
CPU core	Number of instructions	340				
	Minimum execution time	62.5 ns at 4 MHz (PLL: with multiply-by-4 setting)				
	RAM size	1.64 Kbytes	2 Kbytes	3 Kbytes		
	ROM size	32 Kbytes (internal mask ROM)	48 Kbytes (internal mask ROM)	64 Kbytes (internal mask ROM)	None	64 Kbytes (internal OTPROM)
	System clock oscillation circuit	System clock/PLL clock on chip				
	Low-power consumption modes	Sleep, stop, CPU intermittent operation, pseudo-watch, hardware standby				
	Interrupts	Interrupt sources: 19 channels; priority levels: 8 (programmable); external interrupt inputs: 4 channels				
Resources	Ports	Output ports (N-channel open drain): 10 I/O ports (CMOS): 74 Total: 84				
	UART0	8 bits × 1 channel				
	UART1 (SCI)	8 bits × 1 channel				
	A/D converter	10-bit resolution × 8 channels				
	24-bit free-run timer	24 bits × 1 channel				
	ICU (input capture)	24 bits × 4 channels				
	OCU (output compare)	24 bits × 8 channels				
	8-bit PPG timer	8 bits × 2 channels				
	16-bit reload timer	16 bits × 2 channels				
	I^2C interface	8 bits × 1 channel				
	Watchdog timer function	On chip				
Characteristics	Power supply voltage	+2.7 V to +5.5 V				
	Operating temperature	–40°C to +85°C				
	System clock frequency	32 MHz (+5.0 V ± 10%) 16 MHz (+3.0 V ± 10%)				
Miscellaneous	Package	FPT-100P-M05/FPT-100P-M06				
	Process	CMOS				

MB90670/675 Series

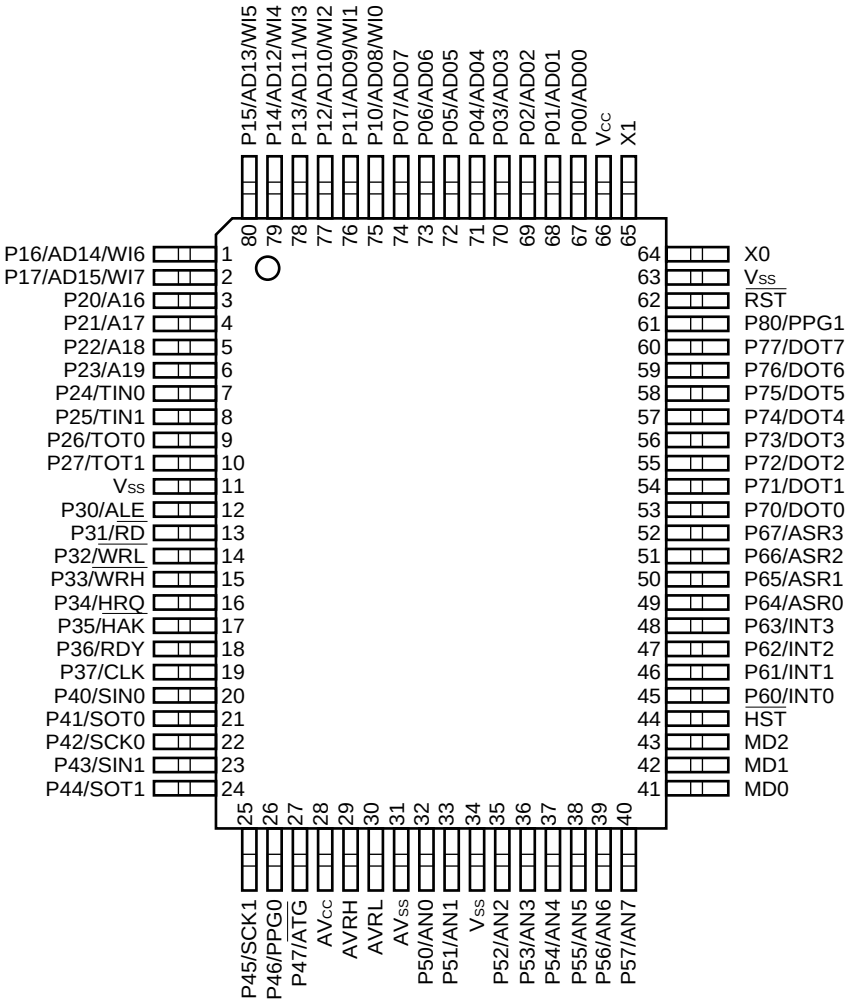
■ PIN ASSIGNMENT

(Top view)



MB90671/672/673/P673/T673
(FPT-80P-M05)

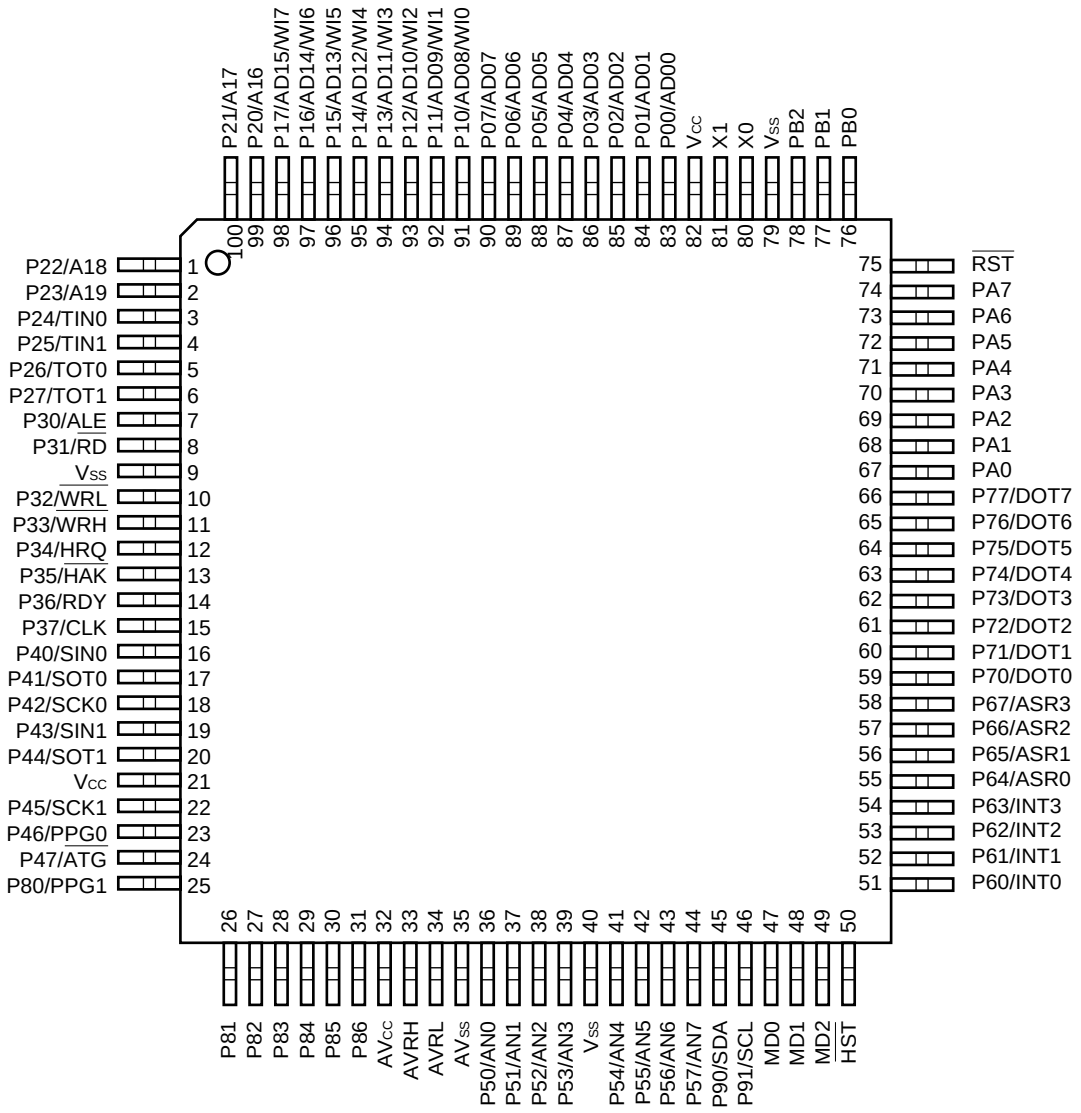
(Top view)



MB90671/672/673/P673/T673
(FPT-80P-M06)

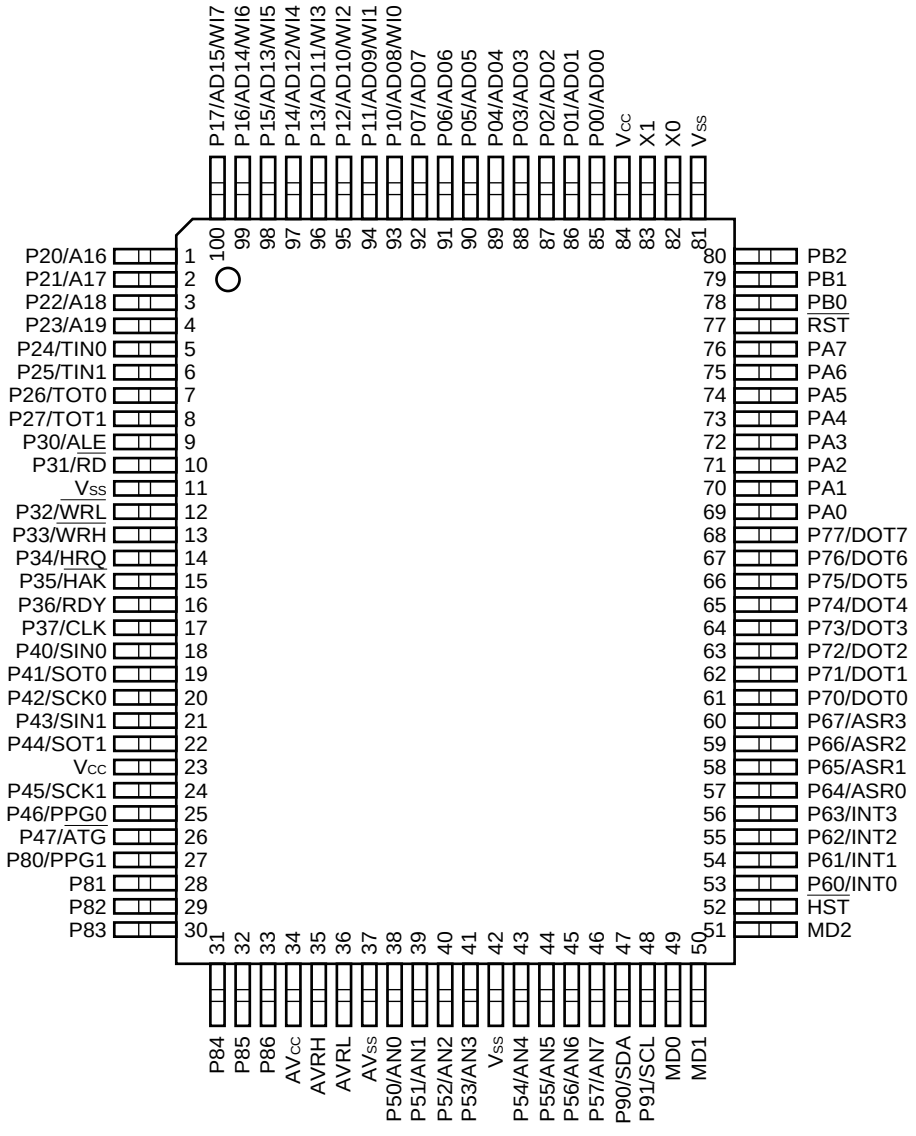
MB90670/675 Series

(Top view)



MB90676/677/678/P678/T678
(FPT-100P-M05)

(Top view)



MB90676/677/678/P678/T678
(FPT-100P-M06)

MB90670/675 Series

■ PIN DESCRIPTION

Pin no.				Pin name	Circuit type	Function
LQFP*1	QFP*2	LQFP*3	QFP*4			
62	64	80	82	X0	A (Oscillation)	Crystal oscillator pins
63	65	81	83	X1		
65 to 72	67 to 74	83 to 90	85 to 92	P00 to P07	B (CMOS)	General-purpose I/O ports This function is valid in single-chip mode.
				AD00 to AD07		I/O pins for the lower 8 bits of the external address/ data bus This function is valid in modes where the external bus is enabled.
73 to 80	75 to 80, 1, 2	91 to 98	93 to 100	P10 to P17	B (CMOS)	General-purpose I/O ports This function is valid in single-chip mode.
				AD08 to AD15		I/O pins for the upper 8 bits of the external address/ data bus This function is valid in modes where the external bus is enabled.
				WI0 to WI7		Wake-up interrupt I/O pins This function is valid in single-chip mode. When external interrupts are enabled, external interrupt inputs may be used at any time. It is necessary to stop port output when external interrupt inputs, except using port output deliberately.
1 to 4	3 to 6	99, 100, 1, 2	1 to 4	P20 to P23	B (CMOS)	General-purpose I/O ports This function is valid either in single-chip mode or when the external address output control register specification is “port.”
				A16 to A19		External address bus output pins A16 to A19 This function is valid in modes where the external bus is enabled and the upper address control register specification is “address.”
5, 6	7, 8	3, 4	5, 6	P24, P25	E (CMOS/H)	General-purpose I/O ports This function is always valid.
				TIN0, TIN1		Reload timer 0 and 1 event input pins During reload timer input operations, reload timer inputs may be used at any time. It is necessary to stop port output when reload timer inputs, except using port output deliberately.
7, 8	9, 10	5, 6	7, 8	P26, P27	E (CMOS/H)	General-purpose I/O ports This function is valid when the reload timer 0 and 1 output is disabled.
				TOT0, TOT1		Reload timer 0 and 1 output pins This function is valid when the reload timer 0 and 1 output is enabled.

*1: FPT-80P-M05
*2: FPT-80P-M06
*3: FPT-100P-M05
*4: FPT-100P-M06

(Continued)

Pin no.				Pin name	Circuit type	Function
LQFP*1	QFP*2	LQFP*3	QFP*4			
10	12	7	9	P30	B (CMOS)	General-purpose I/O port This function is valid in single-chip mode.
				ALE		Address latch enable output pin This function is valid in modes where the external bus is enabled.
11	13	8	10	P31	B (CMOS)	General-purpose I/O port This function is valid in single-chip mode.
				$\overline{RD}$		Read strobe output pin for the data bus This function is valid in modes where the external bus is enabled.
12	14	10	12	P32	B (CMOS)	General-purpose I/O port This function is valid in single-chip mode or when $\overline{WRL}$ pin output is disabled.
				$\overline{WRL}$		Write strobe output pin for the lower eight bits of the data bus This function is valid in modes where the external bus is enabled and $\overline{WRL}$ pin output is enabled.
13	15	11	13	P33	B (CMOS)	General-purpose I/O port This function is valid in single-chip mode, external bus eight-bit mode, or when $\overline{WRH}$ pin output is disabled.
				$\overline{WRH}$		Write strobe output pin for the upper eight bits of the data bus This function is valid in modes where the external bus 16-bit mode is enabled, and $\overline{WRH}$ pin output is enabled.
14	16	12	14	P34	B (CMOS)	General-purpose I/O port This function is valid in single-chip mode and when the hold function is disabled.
				HRQ		Hold request input pin This function is valid in a mode where the external bus is enabled and the hold function is enabled.
15	17	13	15	P35	B (CMOS)	General-purpose I/O port This function is valid in single-chip mode and when the hold function is disabled.
				$\overline{HAK}$		Hold acknowledge output pin This function is valid in a mode where the external bus is enabled and the hold function is enabled.
16	18	14	16	P36	B (CMOS)	General-purpose I/O port This function is valid in single-chip mode and when the external ready function is disabled.
				RDY		Ready input pin This function is valid in a mode where the external bus is enabled and the external ready function is enabled.

*1: FPT-80P-M05
*2: FPT-80P-M06
*3: FPT-100P-M05
*4: FPT-100P-M06

(Continued)

Pin no.				Pin name	Circuit type	Function
LQFP*1	QFP*2	LQFP*3	QFP*4			
17	19	15	17	P37	B (CMOS)	General-purpose I/O port This function is valid in single-chip mode and when the CLK output is disabled.
				CLK		CLK output pin This function is valid in a mode where the external bus is enabled and the CLK output is enabled.
18	20	16	18	P40	E (CMOS/H)	General-purpose I/O port This function is always valid.
				SIN0		UART0 serial data input pin During UART0 input operations, UART0 inputs may be used at any time. It is necessary to stop port output when UART0 inputs, except using port output deliberately.
19	21	17	19	P41	E (CMOS/H)	General-purpose I/O port This function is valid when the UART0 serial data output is disabled.
				SOT0		UART0 serial data output pin This function is valid when the UART0 serial data output is enabled.
20	22	18	20	P42	E (CMOS/H)	General-purpose I/O port This function is valid when the UART0 clock output is disabled.
				SCK0		UART0 clock I/O pin This function is valid when the UART0 clock output is enabled. During UART0 input operations, UART0 inputs may be used at any time. It is necessary to stop port output when UART0 inputs, except using port output deliberately.
21	23	19	21	P43	E (CMOS/H)	General-purpose I/O port This function is always valid.
				SIN1		UART1 serial data input pin During UART1 input operations, UART1 inputs may be used at any time. It is necessary to stop port output when UART1 inputs, except using port output deliberately.
22	24	20	22	P44	E (CMOS/H)	General-purpose I/O port This function is valid when the UART1 serial data output is disabled.
				SOT1		UART1 serial data output pin This function is valid when the UART1 serial data output is enabled.

*1: FPT-80P-M05
*2: FPT-80P-M06
*3: FPT-100P-M05
*4: FPT-100P-M06

(Continued)

Pin no.				Pin name	Circuit type	Function
LQFP*1	QFP*2	LQFP*3	QFP*4			
23	25	22	24	P45	E (CMOS/H)	General-purpose I/O port This function is valid when the UART1 clock output is disabled.
				SCK1		UART1 clock I/O pin During UART1 input operations, UART1 inputs may be used at any time. It is necessary to stop port output when UART1 inputs, except using port output deliberately.
24	26	23	25	P46	E (CMOS/H)	General-purpose I/O port This function is valid when the PPG timer 0 waveform output is disabled.
				PPG0		PPG timer 0 output pin This function is valid when the PPG timer 0 waveform output is enabled.
25	27	24	26	P47	E (CMOS/H)	General-purpose I/O port This function is always valid.
				$\overline{ATG}$		A/D converter trigger input pin During A/D converter input operations, A/D converter inputs may be used at any time. It is necessary to stop port output when A/D converter inputs, except using port output deliberately.
26	28	32	34	AV_{CC}	Power supply	Analog circuit power supply pin This power supply must only be turned on or off when electric potential of AV_{CC} or greater is applied to V_{CC}.
27	29	33	35	AVRH	Power supply	Analog circuit reference voltage input pin This pin must only be turned on or off when electric potential of AVRH or greater is applied to AV_{CC}.
28	30	34	36	AVRL	Power supply	Analog circuit reference voltage input pin
29	31	35	37	AV_{SS}	Power supply	Analog circuit power supply (GND) pin
30, 31, 33 to 38	32, 33, 35 to 40	36 to 39, 41 to 44	38 to 41, 43 to 46	P50 to P57	C (CMOS/N-ch open-drain)	Open-drain type I/O ports The input function is valid when the analog input enable register specification is “port”.
				AN0 to AN7		A/D converter analog input pins This function is valid when the analog input enable register specification is “AD”.
39 to 41	41 to 43	47 to 49	49 to 51	MD0 to MD2	F (CMOS)	Operating mode selection input pins Connect directly to V_{CC} or V_{SS}.
42	44	50	52	$\overline{HST}$	G (H)	Hardware standby input pin

*1: FPT-80P-M05
*2: FPT-80P-M06
*3: FPT-100P-M05
*4: FPT-100P-M06

(Continued)

Pin no.				Pin name	Circuit type	Function
LQFP*1	QFP*2	LQFP*3	QFP*4			
43 to 46	45 to 48	51 to 54	53 to 56	P60 to P63	E (CMOS/H)	General-purpose I/O ports This function is always valid.
				INT0 to INT3		External interrupt request input pins When external interrupts are enabled, external interrupt inputs may be used at any time. It is necessary to stop port output when external interrupt inputs, except using port output deliberately.
47 to 50	49 to 52	55 to 58	57 to 60	P64 to P67	E (CMOS/H)	General-purpose I/O ports This function is always valid.
				ASR0 to ASR3		ICU0 to 3 data sample input pins During ICU operations, ICU inputs may be used at any time. It is necessary to stop port output when ICU inputs, except using port output deliberately.
51 to 58	53 to 60	59 to 66	61 to 68	P70 to P77	E (CMOS/H)	General-purpose I/O ports This function is valid when the OCU waveform output is disabled.
				DOT0 toDOT7		OCU0 and 1 waveform output pins This function is valid when the OCU waveform output is enabled and the port output is set.
59	61	25	27	P80	E (CMOS/H)	General-purpose I/O port This function is valid when the PPG timer 1 waveform output is disabled.
				PPG1		PPG timer 1 output pin This function is valid when the PPG timer 1 waveform output is enabled.
60	62	75	77	$\overline{RST}$	H (CMOS/H)	External reset request input pin
64	66	21, 82	23, 84	V_{CC}	Power supply	Digital circuit power supply pin
9, 32, 61	11, 34, 63	9, 40, 79	11, 42, 81	V_{SS}	Power supply	Digital circuit power supply (GND) pin
—	—	26 to 31	28 to 33	P81 to P86	E (CMOS/H)	General-purpose I/O ports This function is always valid.
—	—	45	47	P90	D (NMOS/H)	Open-drain type I/O port This function is always valid.
				SDA		I^2C interface data I/O pin This function is valid when I^2C interface operations are enabled. Set port output to high impedance (PDR = 1) during I^2C interface operations.

*1: FPT-80P-M05
*2: FPT-80P-M06
*3: FPT-100P-M05
*4: FPT-100P-M06

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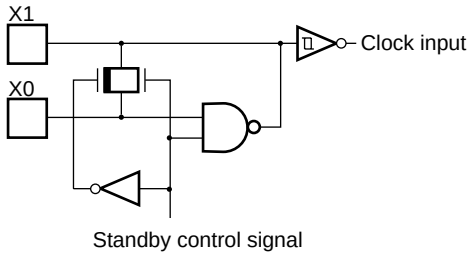
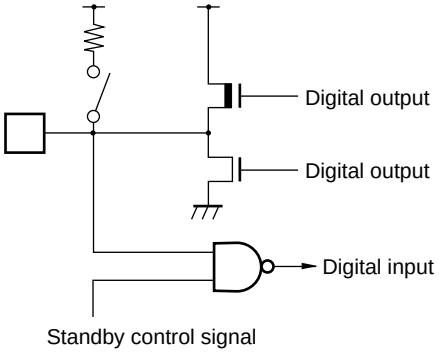
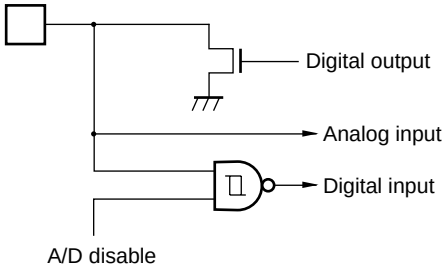
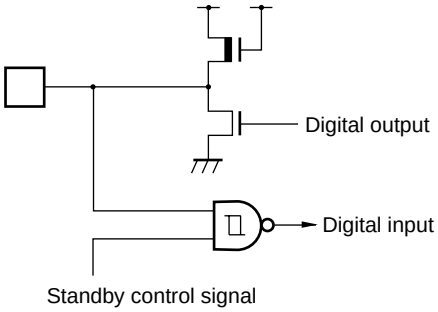
Pin no.				Pin name	Circuit type	Function
LQFP*1	QFP*2	LQFP*3	QFP*4			
—	—	46	48	P91	D (NMOS/H)	Open-drain type I/O port This function is always valid.
				SCL		I^2C interface clock I/O pin This function is valid when I^2C interface operations are enabled. Set port output to high impedance (PDR = 1) during I^2C interface operations.
—	—	67 to 74	69 to 76	PA0 to PA7	E (CMOS/H)	General-purpose I/O ports This function is always valid.
—	—	76 to 78	78 to 80	PB0 to PB2	E (CMOS/H)	General-purpose I/O ports This function is always valid.

*1: FPT-80P-M05
*2: FPT-80P-M06
*3: FPT-100P-M05
*4: FPT-100P-M06

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• 3 MHz to 32 MHz • Oscillation feedback resistor: approximately 1 MΩ
B		• CMOS-level I/O (with standby control) • Pull-up option selectable (with standby control)
C		• N-ch open-drain output • CMOS-level hysteresis input (with A/D control)
D		• NMOS open-drain output • CMOS-level hysteresis input (with standby control)

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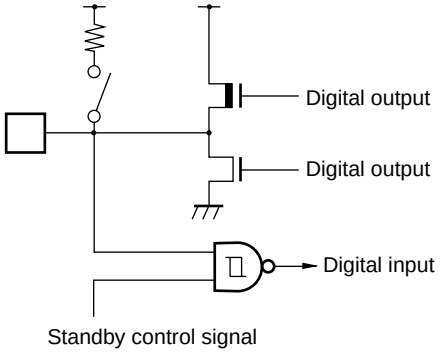
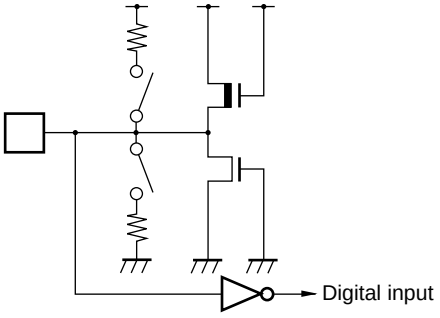
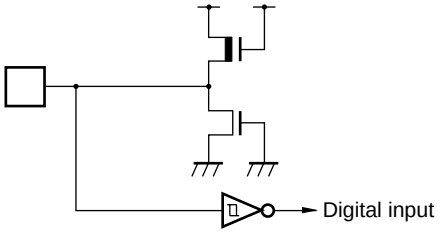
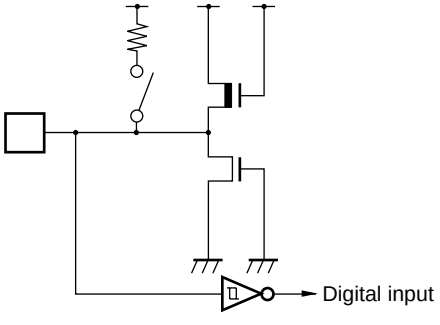
Type	Circuit	Remarks
E		• CMOS-level output • CMOS-level hysteresis input (with standby control) • Pull-up option selectable (with standby control)
F		• CMOS-level input (without standby control) • Pull-up/pull-down option selectable (without standby control) • The MD2 pin has the pull-down resistor selected (this selection is fixed) in the mask ROM version; no option is available for non-mask ROM version.
G		• CMOS-level hysteresis input (without standby control)
H		• CMOS-level hysteresis input (without standby control) • Pull-up option selectable (without standby control)

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to the input or output pins other than medium-and high voltage pins or if higher than the voltage which shown on "■ Absolute Maximum Ratings" is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

In addition, for the same reasons take care to prevent the analog power supply from exceeding the digital power supply.

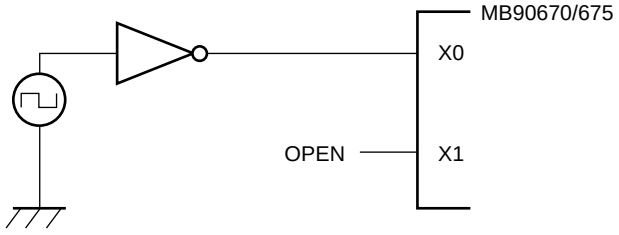
2. Treatment of Unused Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistors.

3. Precautions when Using an External Clock

When an external clock is used, drive X0 only.

Using an External Clock



4. Power Supply Pins

When there are several V_{CC} and V_{SS} pins, those pins that should have the same electric potential are connected within the device when the device is designed in order to prevent misoperation, such as latchup. However, all of those pins must be connected to the power supply and ground externally in order to reduce unnecessary emissions, prevent misoperation of strobe signals due to an increase in the ground level, and to observe the total output current standards.

In addition, give a due consideration to the connection in that current supply be connected to V_{CC} and V_{SS} with the lowest possible impedance.

Finally, it is recommended to connect a capacitor of about 0.1 µF between V_{CC} and V_{SS} near this device as a bypass capacitor.

5. Crystal Oscillation Circuit

Noise in the vicinity of the X0 and X1 pins will cause this device to operate incorrectly. Design the printed circuit board so that the bypass capacitor connecting X0, X1 and the crystal oscillator (or ceramic oscillator) to ground is located as close to the device as possible.

In addition, because printed circuit board artwork in which the area around the X0 and X1 pins is surrounded by ground provides stable operation, such an arrangement is strongly recommended.

6. Sequence for Applying the A/D Converter Power Supply and the Analog Inputs

Always be sure to apply the digital power supply (V_{CC}) before applying the A/D converter power supply (AV_{CC}, AVRH, and AVRL) and the analog inputs (AN0 to AN7).

In addition, when the power is turned off, turn off the A/D converter power supply and the analog inputs first, and then turn off the digital power supply.

Whether applying or cutting off the power, be certain that AVRH does not exceed AV_{CC}. (Turning on or off the analog and digital power supplies simultaneously will not cause any problems.)

7. "MOV @AL, AH" and "MOVW @AL, AH" Instructions

When the above instructions are used in the I/O space, an unnecessary write (#FF, #FFFF) may be performed on the internal bus. This problem can be avoided by using a function that causes the compiler/assembler to generate an NOP immediately before either the above instructions. This problem does not arise when accessing the RAM space.

■ PROGRAMMING TO THE OTPROM ON THE MB90P673/P678

In EPROM mode, the MB90P673/P678 OTPROM functions equivalent to the MBM27C1000. This allows the PROM to be programmed with a general-purpose EPROM programmer by using the dedicated socket adapter.

However, the MB90P673/P678 does not support electronic signature (device identification code) mode.

1. EPROM Programmer Socket Adapter and Recommended Programmer Manufacturer

Part no.	Package	Compatible socket adapter Sun Hayato Co., Ltd.	Minato Electronics Inc.			Data I/O Co., Ltd.		
			1890A	1891	1930	UNSITE	3900	2900
MB90P673PF	QFP-80	ROM-80QF-32DP-16L	—			—		
MB90P673PFV	SQFP-80	ROM-80SQF-32DP-16L	—			—		
MB90P678PF	QFP-100	ROM-100QF-32DP-16L	—			—		
MB90P678PFV	SQFP-100	ROM-100SQF-32DP-16L	Recommended			Recommended		

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106

Minato Electronics Inc.: TEL: USA (1)-916-348-6066
JAPAN (81)-45-591-5611

Data I/O Co., Ltd.: TEL: USA/ASIA (1)-206-881-6444
EUROPE (49)-8-985-8580

2. EPROM Mode Pin Assignments

- **MBM27C1000 compatible pins**

MBM27C1000		MB90P673/MB90P678	
Pin no.	**Pin name**	**Pin no.**	**Pin name**
1	V_{PP}	See “Pin Assignment.”	MD2
2	$\overline{OE}$		P32
3	A15		P17
4	A12		P14
5	A07		P27
6	A06		P26
7	A05		P25
8	A04		P24
9	A03		P23
10	A02		P22
11	A01		P21
12	A00		P20
13	D00		P00
14	D01		P01
15	D02		P02
16	GND		V_{SS}

MBM27C1000		MB90P673/MB90P678	
Pin no.	**Pin name**	**Pin no.**	**Pin name**
32	V_{CC}	See “Pin Assignment.”	V_{CC}
31	$\overline{PGM}$		P33
30	N.C.		—
29	A14		P16
28	A13		P15
27	A08		P10
26	A09		P11
25	A11		P13
24	A16		P30
23	A10		P12
22	$\overline{CE}$		P31
21	D07		P07
20	D06		P06
19	D05		P05
18	D04		P04
17	D03		P03

• **Non-MBM27C1000 compatible pins**

Pin no.	Pin name	Treatment
See “Pin Assignment.”	MD0 MD1 X0	Connect a pull-up resistor of 4.7 kΩ.
	X1	OPEN
	AV_{CC} AVRH P37 P40 to P47 P50 to P57 P60 to P67 P70 to P77 P80 to P86 P90 P91 PA0 to PA7 PB0 to PB2	Connect a pull-up resistor of about 1 MΩ to each pin.

• **Power supply, GND connection pins**

Classification	Pin no.	Pin name
Power supply	See “Pin Assignment.”	$\overline{HST}$ V_{CC}
GND	See “Pin Assignment.”	P34 P35 P36 $\overline{RST}$ AVRL AV_{SS} V_{SS}

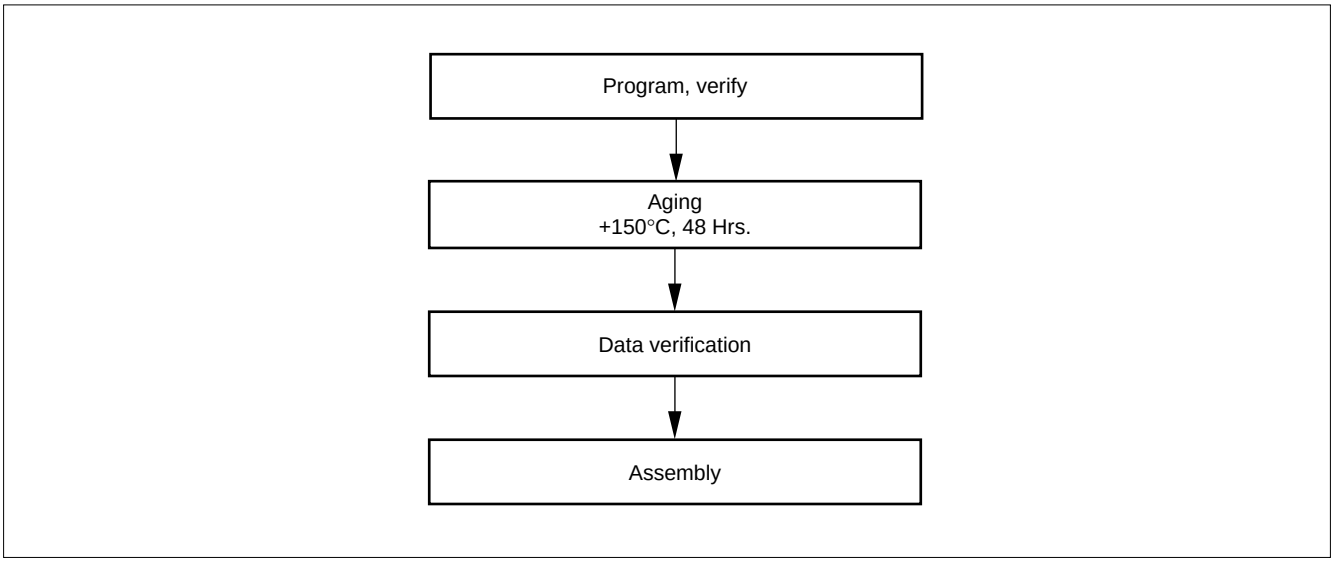
Note: P81 to P86, P90, P91, PA0 to PA7, and PB0 to PB2 are found only in the MB90675 series.

3. Program Mode

In the MB90P673/P678, all of the bits are set to “1” when the IC is shipped from Fujitsu and after erasure. To input data, program the IC by selectively setting the desired bits to “0”. Bits cannot be set to “1” electrically.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM with microcontroller program.



5. Programming Yield

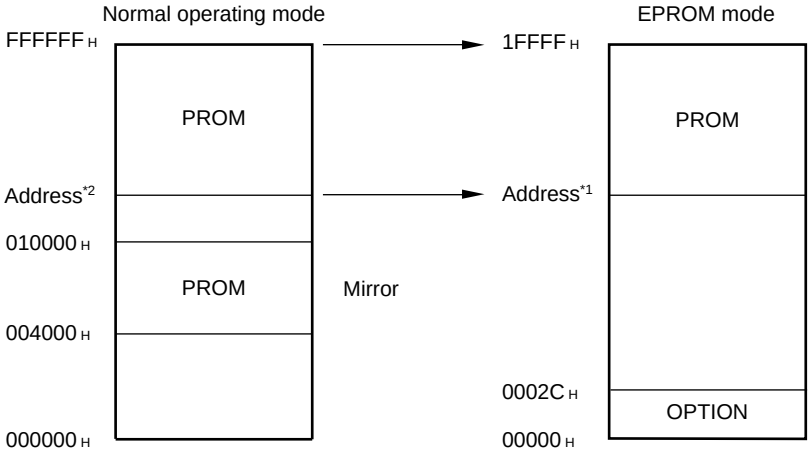
All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. Programming Procedure

(1) Set the EPROM programmer to the MBM27C1000.

(2) Load the program data into the EPROM programmer at address*1 to 1FFFF$_H$. (The ROM addresses from address*2 to FFFFFF$_H$ in normal operating mode correspond to address*1 to 1FFFF$_H$ in EPROM mode.) When specifying option data, load the data into the addresses specified “7, PROM Option Bitmap.”

The memory space for EPROM mode is diagrammed below.



Product	Address *1	Address *2	Number of bytes
MB90P673	14000$_H$	FF4000$_H$	48 Kbytes
MB90P678	10000$_H$	FF0000$_H$	64 Kbytes

The 00 bank PROM mirror is 48 Kbytes. (This is a mirror for FF4000$_H$ to FFFFFF$_H$.)

(3) Insert the MB90P673/P678 in the socket adapter, and mount the socket adapter on the EPROM programmer. Pay attention to the orientation of the device and of the socket adapter when doing so.

(4) Activate the programming.

Notes: • Because the mask ROM products (MB90671/672/673/676/677/678) do not have an EPROM mode, they cannot read data from the EPROM programmer.
• Contact the sales department when purchasing an EPROM programmer.

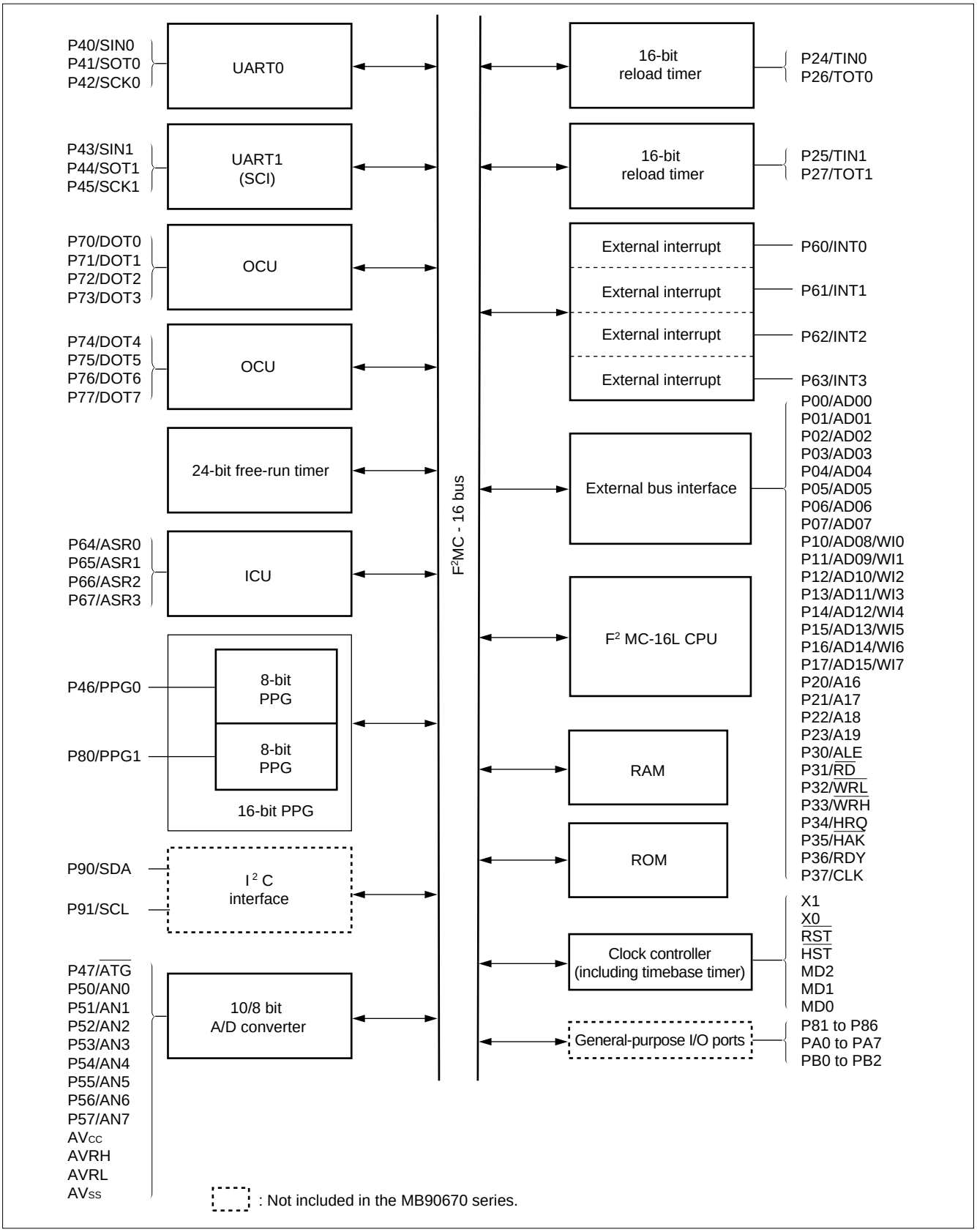
7. OTPROM Option Bitmap

Address \ Bit	7	6	5	4	3	2	1	0
00000H	Vacancy	$\overline{\text{RST}}$ Pull-up 1: No 0: Yes	Vacancy	MD1 Pull-up 1: No 0: Yes	MD1 Pull-down 1: No 0: Yes	MD0 Pull-up 1: No 0: Yes	MD0 Pull-down 1: No 0: Yes	Vacancy
00004H	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
00008H	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
0000CH	P27 Pull-up 1: No 0: Yes	P26 Pull-up 1: No 0: Yes	P25 Pull-up 1: No 0: Yes	P24 Pull-up 1: No 0: Yes	P23 Pull-up 1: No 0: Yes	P22 Pull-up 1: No 0: Yes	P21 Pull-up 1: No 0: Yes	P20 Pull-up 1: No 0: Yes
00010H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
00014H	P47 Pull-up 1: No 0: Yes	P46 Pull-up 1: No 0: Yes	P45 Pull-up 1: No 0: Yes	P44 Pull-up 1: No 0: Yes	P43 Pull-up 1: No 0: Yes	P42 Pull-up 1: No 0: Yes	P41 Pull-up 1: No 0: Yes	P40 Pull-up 1: No 0: Yes
0001CH	P67 Pull-up 1: No 0: Yes	P66 Pull-up 1: No 0: Yes	P65 Pull-up 1: No 0: Yes	P64 Pull-up 1: No 0: Yes	P63 Pull-up 1: No 0: Yes	P62 Pull-up 1: No 0: Yes	P61 Pull-up 1: No 0: Yes	P60 Pull-up 1: No 0: Yes
00020H	P77 Pull-up 1: No 0: Yes	P76 Pull-up 1: No 0: Yes	P75 Pull-up 1: No 0: Yes	P74 Pull-up 1: No 0: Yes	P73 Pull-up 1: No 0: Yes	P72 Pull-up 1: No 0: Yes	P71 Pull-up 1: No 0: Yes	P70 Pull-up 1: No 0: Yes
00024H	Vacancy	P86 Pull-up 1: No 0: Yes	P85 Pull-up 1: No 0: Yes	P84 Pull-up 1: No 0: Yes	P83 Pull-up 1: No 0: Yes	P82 Pull-up 1: No 0: Yes	P81 Pull-up 1: No 0: Yes	P80 Pull-up 1: No 0: Yes
00028H	PA5 Pull-up 1: No 0: Yes	PA4 Pull-up 1: No 0: Yes	PA3 Pull-up 1: No 0: Yes	PA2 Pull-up 1: No 0: Yes	PA1 Pull-up 1: No 0: Yes	PA0 Pull-up 1: No 0: Yes	Vacancy	Vacancy
0002CH	Vacancy	Vacancy	Vacancy	PB2 Pull-up 1: No 0: Yes	PB1 Pull-up 1: No 0: Yes	PB0 Pull-up 1: No 0: Yes	PA7 Pull-up 1: No 0: Yes	PA6 Pull-up 1: No 0: Yes

Notes:
- Do not write “0” to the vacant bits and for addresses other than those indicated above.
- The pull-up option for P81 to P86, PA0 to PA7, and PB0 to PB2 exists only for the MB90P678. Write “1” to these bits in the MB90P673.

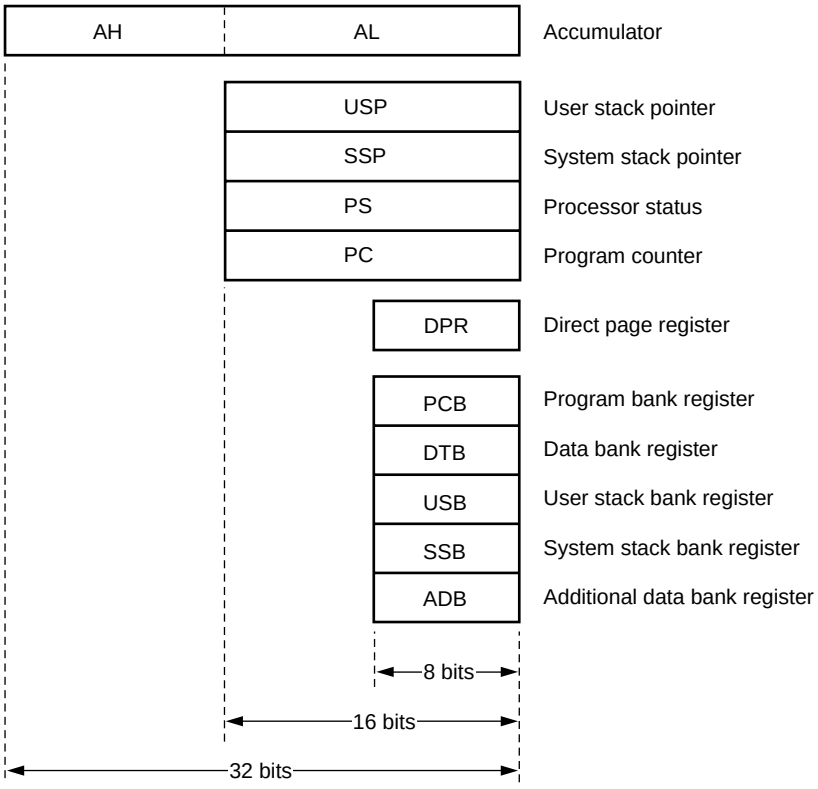
MB90670/675 Series

■ BLOCK DIAGRAM

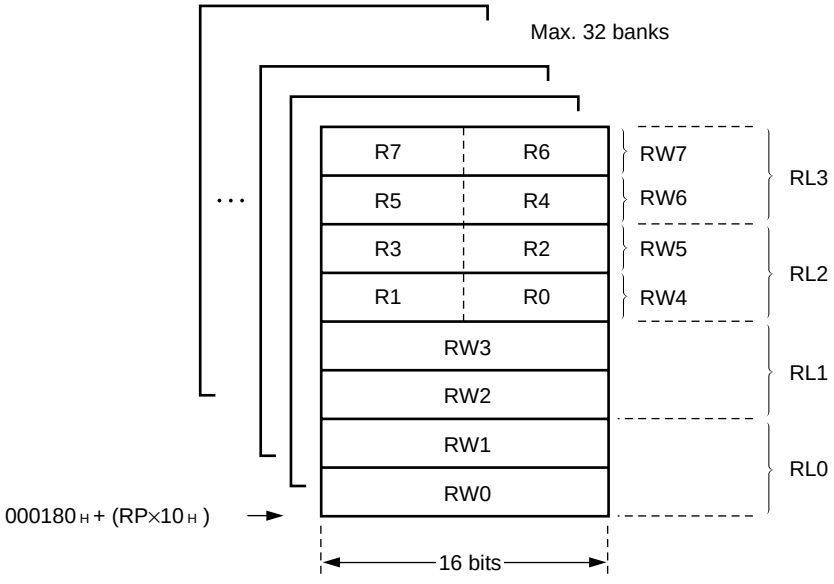


■ F²MC-16L CPU PROGRAMMING MODEL

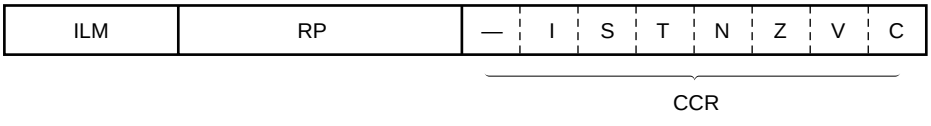
• **Dedicated Registers**



• **General-purpose Registers**

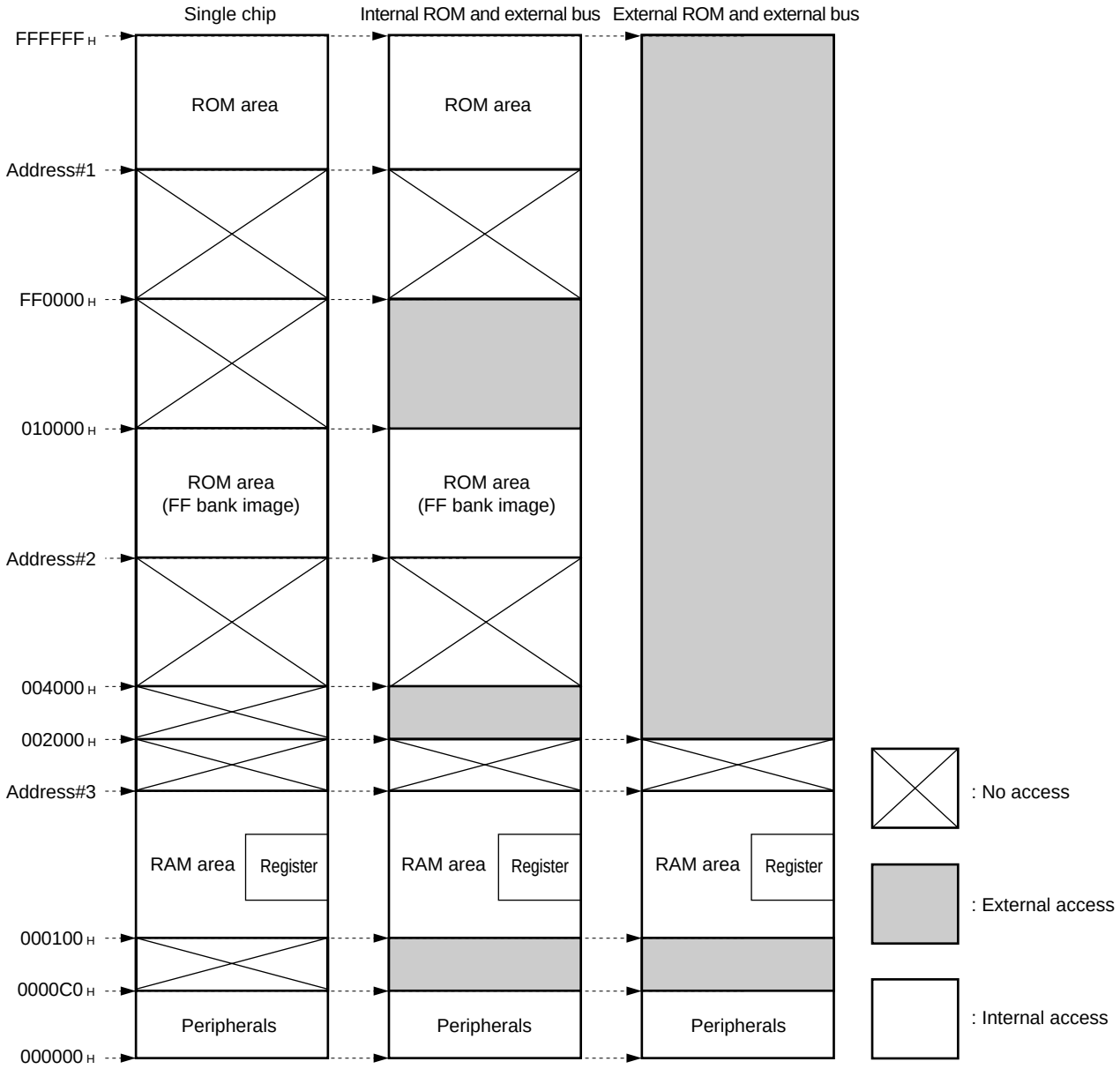


• **Processor Status (PS)**



MB90670/675 Series

■ MEMORY MAP



Product	Address #1	Address #2	Address #3
MB90671	FFC000H	00C000H	000380H
MB90672	FF8000H	008000H	000780H
MB90673/P673	FF4000H	004000H	000900H
MB90676	FF8000H	008000H	000780H
MB90677	FF4000H	004000H	000900H
MB90678/P678	FF0000H	004000H	000D00H

Notes:
- While the ROM data image of bank FF can be seen in the upper portion of bank 00, this is done only to permit effective use of the C compiler's small model. Because the lower 16 bits are the same, it is possible to reference tables in ROM without declaring the "far" specification in the pointer.
  However, because the ROM area in the MB90678/P678 exceeds 48 Kbytes, the image for $FF4000_H$ to $FFFFFF_H$ can be seen in bank 00, while $FF0000_H$ to $FF3FFF_H$ can only be seen in bank FF.

- In the MB90670/675 series, the upper four bits of addresses are not output to the external bus. As a result, the maximum memory space that can actually be accessed is 1MB. In addition, the same address is accessed by image at the address in a different bank.

- In order to prevent the contents of memory and I/O from being destroyed when accessed by image, it is recommended that programs be written so that the number of banks accessed by the external bus be limited to 16 with different addresses.
  Note that this same situation arises even when masking upper addresses through the external address output control register.

■ I/O MAP

Address	Register	Register name	Access*7	Resource name	Initial value
000000H	Port 0 data register	PDR0	R/W	Port 0	XXXXXXXX
000001H	Port 1 data register	PDR1	R/W	Port 1	XXXXXXXX
000002H	Port 2 data register	PDR2	R/W	Port 2	XXXXXXXX
000003H	Port 3 data register	PDR3	R/W	Port 3	XXXXXXXX
000004H	Port 4 data register	PDR4	R/W	Port 4	XXXXXXXX
000005H	Port 5 data register	PDR5	R/W	Port 5	11111111
000006H	Port 6 data register	PDR6	R/W	Port 6	XXXXXXXX
000007H	Port 7 data register	PDR7	R	Port 7	XXXXXXXX
000008H	Port 8 data register	PDR8	R/W	Port 8*5	–XXXXXXX
000009H	Port 9 data register	PDR9	R/W	Port 9*5	––––––11
00000AH	Port A data register	PDRA	R/W	Port A*5	XXXXXXXX
00000BH	Port B data register	PDRB	R/W	Port B*5	–––––XXX
00000CH to 0EH	Vacancy	—	*3	—	—
00000FH	Wake-up interrupt flag register	EIFR	R/W	Wake-up interrupt	––––––––0
000010H	Port 0 direction register	DDR0	R/W	Port 0	00000000
000011H	Port 1 direction register	DDR1	R/W	Port 1	00000000
000012H	Port 2 direction register	DDR2	R/W	Port 2	00000000
000013H	Port 3 direction register	DDR3	R/W	Port 3	00000000
000014H	Port 4 direction register	DDR4	R/W	Port 4	00000000
000015H	Analog input enable register	ADER	R/W	Port 5	11111111
000016H	Port 6 direction register	DDR6	R/W	Port 6	00000000
000017H	Port 7 direction register	DDR7	R/W	Port 7	00000000
000018H	Port 8 direction register	DDR8	R/W	Port 8*5	–0000000
000019H	Vacancy	—	—	—	—
00001AH	Port A direction register	DDRA	R/W	Port A*5	00000000
00001BH	Port B direction register	DDRB	R/W	Port B*5	–––––000
00001CH to 1EH	Vacancy	—	*3	—	—
00001FH	Wake-up interrupt enable register	EICR	W	Wake-up interrupt	00000000
000020H	Mode control register 0	UMC	R/W!	UART0	00000100
000021H	Status register 0	USR	R/W!		00010000
000022H	Input data register 0/ output data register 0	UIDR /UODR	R/W		XXXXXXXX
000023H	Rate and data register 0	URD	R/W		00000000

(Continued)

Address	Register	Register name	Access*7	Resource name	Initial value
000024H	Serial mode register 1	SMR	R/W	UART1 (SCI)	00000000
000025H	Serial control register 1	SCR	R/W!		00000100
000026H	Serial input data register 1/ Serial output data register 1	SIDR/ SODR	R/W		XXXXXXXX
000027H	Serial status register 1	SSR	R/W!		00001–00
000028H	Interrupt/DTP enable register	ENIR	R/W	DTP/external interrupt	–––00000
000029H	Interrupt/DTP source register	EIRR	R/W		–––00000
00002AH	Request level setting register	ELVR	R/W		00000000
00002BH	Vacancy	—	—	—	—
00002CH	A/D converter control status register	ADCS	R/W!	A/D converter	00000000
00002DH					00000000
00002EH	A/D converter data register	ADCR	R/W! *4		XXXXXXXX
00002FH					000000XX
000030H	PPG0 operating mode control register	PPGC0	R/W	PPG0	0–000001
000031H	PPG1 operating mode control register	PPGC1	R/W	PPG1	00000001
000032H to 33H	Vacancy	—	*3	—	—
000034H	PPG0 reload register	PRLL0/ PRLH0	R/W	PPG0	XXXXXXXX
000035H					XXXXXXXX
000036H	PPG1 reload register	PRLL1/ PRLH1	R/W	PPG1	XXXXXXXX
000037H					XXXXXXXX
000038H	Control status register	TMCSR0	R/W!	16-bit reload timer 0	00000000
000039H					––––0000
00003AH	16-bit timer register/16-bit reload register	TMR0/ TMRLR0	R/W		XXXXXXXX
00003BH					XXXXXXXX
00003CH	Control status register	TMCSR1	R/W!	16-bit reload timer 1	00000000
00003DH					––––0000
00003EH	16-bit timer register/16-bit reload register	TMR1/ TMRLR1	R/W		XXXXXXXX
00003FH					XXXXXXXX
000040H	I²C bus status register	IBSR	R	I²C bus IF*6	00000000
000041H	I²C bus control register	IBCR	R/W		00000000
000042H	I²C bus clock selection register	ICCR	R/W		––0XXXXX
000043H	I²C bus address register	IADR	R/W		–XXXXXXX
000044H	I²C bus data register	IDAR	R/W		XXXXXXXX

(Continued)

Address	Register	Register name	Access*7	Resource name	Initial value
000045H to 4FH	Vacancy	—	*3	—	—
000050H	Free-run timer control register	TCCR	R/W!	24-bit free-run timer	11000000
000051H					--111111
000052H	ICU control register	ICC	R/W	ICU	00000000
000053H					00000000
000054H	Free-run timer lower 16-bit data register	TCRL	R	24-bit free-run timer	00000000
000055H					00000000
000056H	Free-run timer upper 16-bit data register	TCRH	R		00000000
000057H					00000000
000058H	OCU control register 00	CCR00	R/W	OCU0	11110000
000059H					----0000
00005AH	OCU control register 01	CCR01	R/W		----0000
00005BH					00000000
00005CH	OCU control register 10	CCR10	R/W	OCU1	11110000
00005DH					----0000
00005EH	OCU control register 11	CCR11	R/W		----0000
00005FH					00000000
000060H	ICU lower data register 0	ICR0L	R	ICU	XXXXXXXX
000061H					XXXXXXXX
000062H	ICU upper data register 0	ICR0H	R		XXXXXXXX
000063H					00000000
000064H	ICU lower data register 1	ICR1L	R		XXXXXXXX
000065H					XXXXXXXX
000066H	ICU upper data register 1	ICR1H	R		XXXXXXXX
000067H					00000000
000068H	ICU lower data register 2	ICR2L	R		XXXXXXXX
000069H					XXXXXXXX
00006AH	ICU upper data register 2	ICR2H	R		XXXXXXXX
00006BH					00000000
00006CH	ICU lower data register 3	ICR3L	R		XXXXXXXX
00006DH					XXXXXXXX

(Continued)

Address	Register	Register name	Access*7	Resource name	Initial value
00006EH	ICU upper data register 3	ICR3H	R	ICU	XXXXXXXX
00006FH					00000000
000070H	OCU compare lower data register 0	CPR00L	R/W	OCU0	00000000
000071H					00000000
000072H	OCU compare upper data register 0	CPR00H	R/W		00000000
000073H					00000000
000074H	OCU compare lower data register 1	CPR01L	R/W		00000000
000075H					00000000
000076H	OCU compare upper data register 1	CPR01H	R/W		00000000
000077H					00000000
000078H	OCU compare lower data register 2	CPR02L	R/W		00000000
000079H					00000000
00007AH	OCU compare upper data register 2	CPR02H	R/W		00000000
00007BH					00000000
00007CH	OCU compare lower data register 3	CPR03L	R/W		00000000
00007DH					00000000
00007EH	OCU compare upper data register 3	CPR03H	R/W		00000000
00007FH					00000000
000080H	OCU compare lower data register 4	CPR04L	R/W	OCU1	00000000
000081H					00000000
000082H	OCU compare upper data register 4	CPR04H	R/W		00000000
000083H					00000000
000084H	OCU compare lower data register 5	CPR05L	R/W		00000000
000085H					00000000
000086H	OCU compare upper data register 5	CPR05H	R/W		00000000
000087H					00000000
000088H	OCU compare lower data register 6	CPR06L	R/W		00000000
000089H					00000000
00008AH	OCU compare upper data register 6	CPR06H	R/W		00000000
00008BH					00000000
00008CH	OCU compare lower data register 7	CPR07L	R/W		00000000
00008DH					00000000

(Continued)

(Continued)

Address	Register	Register name	Access*7	Resource name	Initial value
00008E$_H$	OCU compare upper data register 7	CPR07H	R/W	OCU1	00000000
00008F$_H$					00000000
000090$_H$ to 9E$_H$	System reserved area	—	*1	—	—
00009F$_H$	Delayed interrupt source generation/ release register	DIRR	R/W	Delayed interrupt generation module	–––––––0
0000A0$_H$	Low power consumption mode control register	LPMCR	R/W!	Low-power consumption	00011000
0000A1$_H$	Clock selection register	CKSCR	R/W!	Low-power consumption	11111100
0000A2$_H$ to A4$_H$	Vacancy	—	*3	—	—
0000A5$_H$	Automatic ready function selection register	ARSR	W	External pin	0011––00
0000A6$_H$	External address output control register	HACR	W	External pin	––––0000
0000A7$_H$	Bus control signal selection register	EPCR	W	External pin	0000*00–
0000A8$_H$	Watchdog timer control register	WDTC	R/W!	Watchdog timer	XXXXX111
0000A9$_H$	Timebase timer control register	TBTC	R/W!	Timebase timer	1––00100
0000AA$_H$ to AF$_H$	Vacancy	—	*3	—	—
0000B0$_H$	Interrupt control register 00	ICR00	R/W!	Interrupt controller	00000111
0000B1$_H$	Interrupt control register 01	ICR01	R/W!		00000111
0000B2$_H$	Interrupt control register 02	ICR02	R/W!		00000111
0000B3$_H$	Interrupt control register 03	ICR03	R/W!		00000111
0000B4$_H$	Interrupt control register 04	ICR04	R/W!		00000111
0000B5$_H$	Interrupt control register 05	ICR05	R/W!		00000111
0000B6$_H$	Interrupt control register 06	ICR06	R/W!		00000111
0000B7$_H$	Interrupt control register 07	ICR07	R/W!		00000111
0000B8$_H$	Interrupt control register 08	ICR08	R/W!		00000111
0000B9$_H$	Interrupt control register 09	ICR09	R/W!		00000111
0000BA$_H$	Interrupt control register 10	ICR10	R/W!		00000111
0000BB$_H$	Interrupt control register 11	ICR11	R/W!		00000111
0000BC$_H$	Interrupt control register 12	ICR12	R/W!		00000111
0000BD$_H$	Interrupt control register 13	ICR13	R/W!		00000111
0000BE$_H$	Interrupt control register 14	ICR14	R/W!		00000111
0000BF$_H$	Interrupt control register 15	ICR15	R/W!		00000111
0000C0$_H$ to FF$_H$	External area *2	—	—	—	—

Explanation of initial values

0: The initial value of this bit is “0”.

1: The initial value of this bit is “1”.

*: The initial value of this bit is either “1” or “0”. (The value is determined by the level of the MD0 to 2 pins.)

X: The initial value of this bit is undefined.

–: This bit is not used. No initial value is defined.

*1: Access prohibited.

*2: The only area available for the external access below address 0000FF$_H$ is this area. Accesses to these addresses are handled as accesses to an external I/O area.

*3: Areas labelled “Vacancy” in the I/O map are reserved areas; accesses to these areas are handled accesses to internal areas. No access signal is generated for the external bus.

*4: Only bit 15 can be read. Writes to other bits are used for testing. Reading any bit from bit 10 to 15 returns a “0”.

*5: P81 to P86, P90, P91, PA0 to PA7, and PB0 to PB2 do not exist in the MB90670 series. Therefore, the bits corresponding to these pins are unused.

*6: The I^2C bus interface is not included in the MB90670 series. Therefore, this area is treated as “Vacancy” in the MB90670 series.

*7: Registers for which “R/W!” is indicated in the “Access” column contain some read-only or write-only bits. For details, refer to the “Register configuration” for the resource in question.

Note: For write-only bits, the value to be initialized on reset is described as the initial value. Note that the value of this bit is not the one for reading out.
In addition, the LPMCR, CKSCR, and WDTC may or may not be initialized, depending on the type of reset. The value indicated is the initial value in those cases where the register is initialized.

■ INTERRUPT SOURCES AND THEIR INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS support	Interrupt vector			Interrupt control register	
		No.		Address	ICR	Address
Reset	×	# 08	08H	FFFFDCH	—	—
INT9 instruction	×	# 09	09H	FFFFD8H	—	—
Exception	×	# 10	0AH	FFFFD4H	—	—
External interrupt #0	○	# 11	0BH	FFFFD0H	ICR00	0000B0H
External interrupt #1	○	# 12	0CH	FFFFCCH		
External interrupt #2	○	# 13	0DH	FFFFC8H	ICR01	0000B1H
External interrupt #3	○	# 14	0EH	FFFFC4H		
OCU # 0	○	# 15	0FH	FFFFC0H	ICR02	0000B2H
OCU # 1	○	# 16	10H	FFFFBCH		
OCU # 2	○	# 17	11H	FFFFB8H	ICR03	0000B3H
OCU # 3	○	# 18	12H	FFFFB4H		
OCU # 4	○	# 19	13H	FFFFB0H	ICR04	0000B4H
OCU # 5	○	# 20	14H	FFFFACH		
OCU # 6	○	# 21	15H	FFFFA8H	ICR05	0000B5H
OCU # 7	○	# 22	16H	FFFFA4H		
24-bit free-run timer overflow	○	# 23	17H	FFFFA0H	ICR06	0000B6H
24-bit free-run timer intermediate bit	○	# 24	18H	FFFF9CH		
ICU # 0	○	# 25	19H	FFFF98H	ICR07	0000B7H
ICU # 1	○	# 26	1AH	FFFF94H		
ICU # 2	○	# 27	1BH	FFFF90H	ICR08	0000B8H
ICU # 3	○	# 28	1CH	FFFF8CH		
16-bit reload timer #0/PPG#0	△	# 29	1DH	FFFF88H	ICR09	0000B9H
16-bit reload timer #1/PPG#1	△	# 30	1EH	FFFF84H		
A/D converter measurement complete	○	# 31	1FH	FFFF80H	ICR10	0000BAH
Wake-up interrupt	×	# 33	21H	FFFF78H	ICR11	0000BBH
Time-base timer interval interrupt	×	# 34	22H	FFFF74H		
UART1 transmission complete	○	# 35	23H	FFFF70H	ICR12	0000BCH
UART0 transmission complete	○	# 36	24H	FFFF6CH		
UART1 reception complete	◎	# 37	25H	FFFF68H	ICR13	0000BDH
I²C interface*	×	# 38	26H	FFFF64H		

(Continued)

(Continued)

Interrupt source	EI²OS support	Interrupt vector			Interrupt control register	
		No.		Address	ICR	Address
UART0 reception complete	◎	# 39	27H	FFFF60H	ICR14	0000BEH
Delayed interrupt generation module	×	# 42	2AH	FFFF54H	ICR15	0000BFH

* : Because the MB90670 series does not include the I²C interface, this interrupt vector is not used.

Notes:
- ○ indicates EI²OS support (without stop requests), ◎ indicates EI²OS support (with stop requests), × indicates without EI²OS support, and △ indicates that the 16-bit reload timer supports EI²OS, while the PPG does not.
- Do not set EI²OS startup in an ICRXX that does not support EI²OS.
- Because different interrupt sources share interrupt vector numbers #29 and #30, use the interrupt enable bits in each of the peripherals to select the interrupt source.
- When EI²OS is used for the following sources that share interrupt vector numbers, the interrupt enable bit of each peripheral must be active for only one interrupt source:
  Interrupt number
  16-bit reload timer #0 and PPG#0: #29
  16-bit reload timer #1 and PPG#1: #30

  Note that because PPG does not support EI²OS, the PPG interrupt must be disabled when using EI²OS with the 16-bit reload timer.

■ PERIPHERALS

1. Parallel Ports

(1) I/O Ports

When not being used as output pins by their corresponding peripherals, all pins except for ports 5, 7 and 9 can be individually specified for input or output by setting the corresponding location in the port direction register. When reading a port data register during input, the value is always read as the pin level; when reading a port data register during output, the value latched in the port data register is read. This also applies to the read portion of a read-modify-write operation.

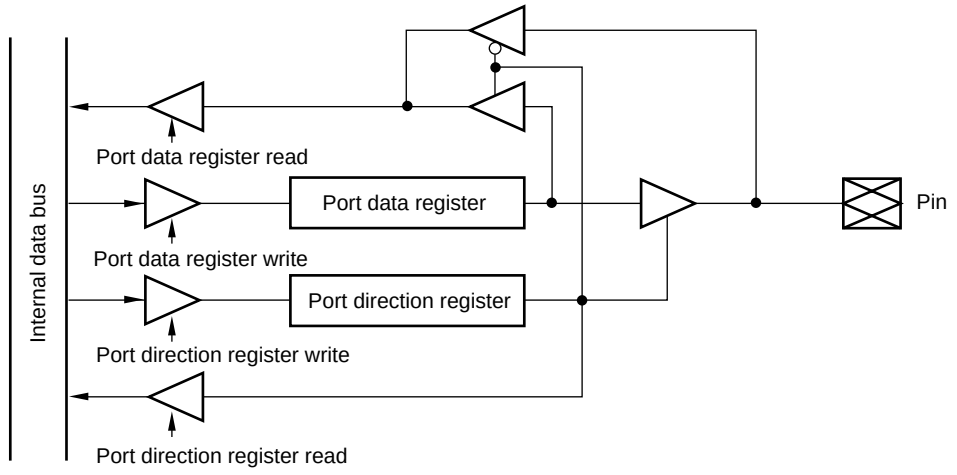
When reading a port data register used as a control output, the data being output as the control output is read, regardless of the value of the port direction register.

If read-modify-write instructions (bit set instruction, etc.) are used to access this register, the bit that is the focus of the instruction is set to the prescribed value, but the contents of the output register corresponding to any other bits for which the input setting has been made are overwritten with the current input value of the corresponding pin. Therefore, when switching a pin that was being used for input over to output, first write the desired value to the port data register, and then write “1” to the port direction register.

Reading and writing an I/O port differs from reading and writing memory as follows:

- Input mode
  Reads: The read data is the level of the corresponding pin.
  Writes: The write data is stored in the output latch. The data is not output to the pin.
- Output mode
  Reads: The read data is the value stored in the PDR.
  Writes: The write data is both stored in the output latch and output to the pin.

- **Block Diagram**



(2) Open-drain Port

Ports 5 and 9 are general-purpose I/O ports with an open-drain output. Port 5 also can serve as an analog input; when port 5 is used as a general-purpose port, always be sure to set the corresponding bits in ADER to “0”. Port 9 also serve as an I²C I/O; when port 9 is used as a general-purpose port, be sure to stop I²C operations.

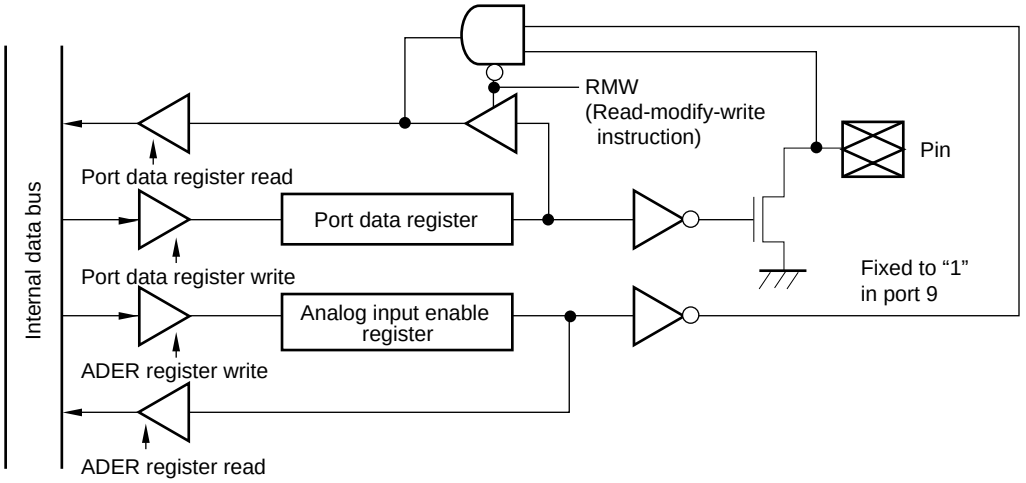
When ports 5 and 9 are used as input ports, it is necessary set the output port data register value to “1” in order to turn off the open drain output transistor; it is also necessary to connect a pull-up resistor to the external pins. In addition, depending on the instruction used to read these bits, one of the following two operations is performed:

- When read by a read-modify-write instruction:
  The contents of the output port data register are read. Even if pins are forcibly set to “0” externally, the contents of the bits not specified by the instruction do not change.
- When read by any other instruction:
  The pin level can be read.

When used as output ports, the pin values can be changed by writing the desired value to the corresponding output port data register.

In addition, a “0” is always read when reading pins corresponding to bits for which a “1” is set in the ADER.

• Block Diagram

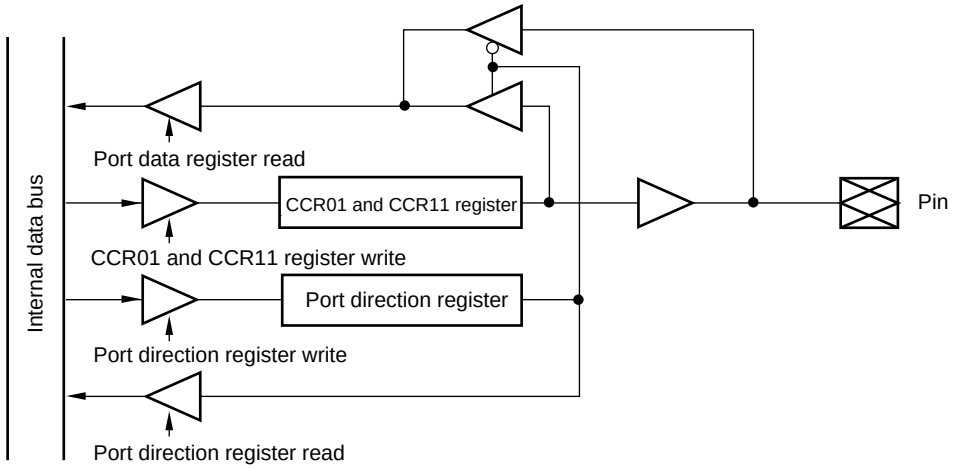


(3) Output Ports

For port 7, when the port direction register is set for output, the value set in DOT0 to 3 bits of CCR01 and CCR11 register of the OCU is output. In addition, the data that is read from the data register in this state is the value being output on the pins.

If the port direction register is set for input, the value set in the DOT0 to 3 bits of CCR01 and CCR11 register of the OCU is not output; the input value on the pin is read.

- **Block Diagram**



(4) Register Configuration

Bit	15/7	14/6	13/5	12/4	11/3	10/2	9/1	8/0	
Address : 000000H	P07	P06	P05	P04	P03	P02	P01	P00	Port 0 data register (PDR0)
Address : 000001H	P17	P16	P15	P14	P13	P12	P11	P10	Port 1 data register (PDR1)
Address : 000002H	P27	P26	P25	P24	P23	P22	P21	P20	Port 2 data register (PDR2)
Address : 000003H	P37	P36	P35	P34	P33	P32	P31	P30	Port 3 data register (PDR3)
Address : 000004H	P47	P46	P45	P44	P43	P42	P41	P40	Port 4 data register (PDR4)
Address : 000005H	P57	P56	P55	P54	P53	P52	P51	P50	Port 5 data register (PDR5)
Address : 000006H	P67	P66	P65	P64	P63	P62	P61	P60	Port 6 data register (PDR6)
Address : 000007H	P77	P76	P75	P74	P73	P72	P71	P70	Port 7 data register (PDR7)
Address : 000008H	–	P86	P85	P84	P83	P82	P81	P80	Port 8 data register (PDR8)
Address : 000009H	–	–	–	–	–	–	P91	P90	Port 9 data register (PDR9)
Address : 00000AH	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Port A data register (PDRA)
Address : 00000BH	–	–	–	–	–	PB2	PB1	PB0	Port B data register (PDRB)

Bit	15/7	14/6	13/5	12/4	11/3	10/2	9/1	8/0	
Address : 000010H	P07	P06	P05	P04	P03	P02	P01	P00	Port 0 direction register (DDR0)
Address : 000011H	P17	P16	P15	P14	P13	P12	P11	P10	Port 1 direction register (DDR1)
Address : 000012H	P27	P26	P25	P24	P23	P22	P21	P20	Port 2 direction register (DDR2)
Address : 000013H	P37	P36	P35	P34	P33	P32	P31	P30	Port 3 direction register (DDR3)
Address : 000014H	P47	P46	P45	P44	P43	P42	P41	P40	Port 4 direction register (DDR4)
Address : 000015H	P57	P56	P55	P54	P53	P52	P51	P50	Analog input enable register (ADER)
Address : 000016H	P67	P66	P65	P64	P63	P62	P61	P60	Port 6 direction register (DDR6)
Address : 000017H	P77	P76	P75	P74	P73	P72	P71	P70	Port 7 direction register (DDR7)
Address : 000018H	–	P86	P85	P84	P83	P82	P81	P80	Port 8 direction register (DDR8)
Address : 00001AH	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Port A direction register (DDRA)
Address : 00001BH	–	–	–	–	–	PB2	PB1	PB0	Port B direction register (DDRB)

Note: P81 to P86, P90, P91, PA0 to PA7, and PB0 to PB2 are provided only in the MB90675 series; they are not available in the MB90670 series.

2. UART0

The UART0 is a serial I/O port used for synchronous or asynchronous communications with external devices; the features of this module are as follows:

- Full-duplex double buffer
- CLK synchronous and CLK asynchronous start-stop data transfers capable
- Supports multiprocessor mode (mode 2)
- Built-in dedicated baud rate generator (12 rates)
- Permits setting of any desired baud rate according to an external clock input or internal timer
- Variable data lengths [7 to 9 bits (no parity), 6 to 8 bits (with parity)]
- Error detection function (framing errors, overrun errors, and parity errors)
- Interrupt functions (two sources: transmission and reception)
- NRZ system as transfer format

(1) Register Configuration

Mode control register 0
Address : channel 0 000020H

	7	6	5	4	3	2	1	0	←Bit no.
	PEN	SBL	MC1	MC0	SMDE	RFC	SCKE	SOE	UMC
Read/write→	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(W)	(R/W)	(R/W)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(1)	(0)	(0)	

Status register 0
Address : channel 0 000021H

	15	14	13	12	11	10	9	8	←Bit no.
	RDRF	ORFE	PE	TDRE	RIE	TIE	RBF	TBF	USR
Read/write→	(R)	(R)	(R)	(R)	(R/W)	(R/W)	(R)	(R)	
Initial value→	(0)	(0)	(0)	(1)	(0)	(0)	(0)	(0)	

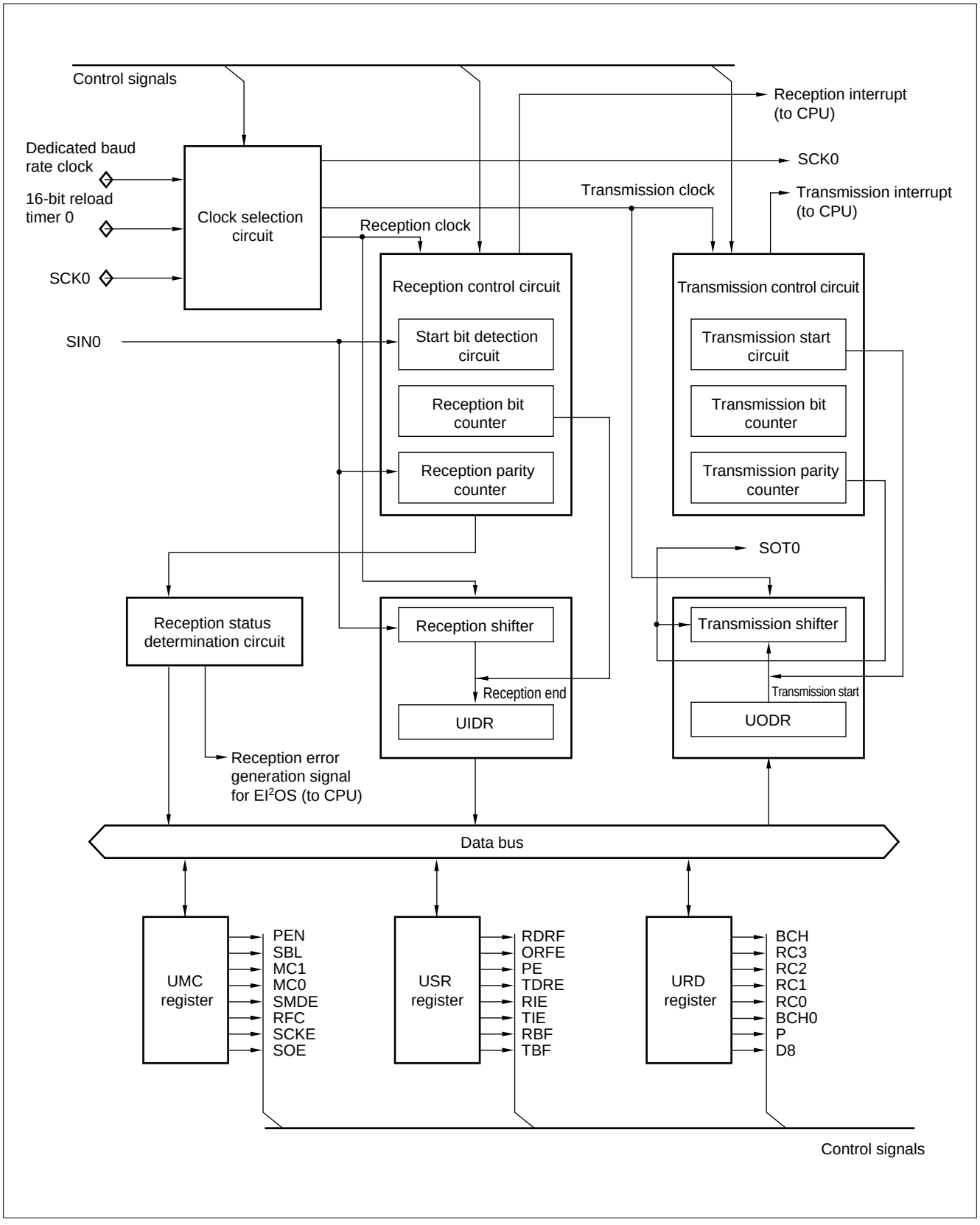
Input data register 0/
output data register 0
Address : channel 0 000022H

	7	6	5	4	3	2	1	0	←Bit no.
	D7	D6	D5	D4	D3	D2	D1	D0	UIDR (read)/ UODR (write)
Read/write→	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value→	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

Rate and data register 0
Address : channel 0 000023H

	15	14	13	12	11	10	9	8	←Bit no.
	BCH	RC3	RC2	RC1	RC0	BCH0	P	D8	URD
Read/write→	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

(2) Block Diagram



3. UART1 (SCI)

The UART is a serial I/O port used for CLK asynchronous (start-stop synchronization) communications or for CLK synchronous (I/O extended serial) communications. The features of this module are described below:

- Full-duplex double buffer
- CLK asynchronous (start-stop synchronization) communications and CLK synchronous (I/O extended serial) communications capable
- Supports multiprocessor mode
- Built-in dedicated baud rate generator
  CLK asynchronous: 62500, 31250, 19230, 9615, 4808, 2404 and 1202 bps
  CLK synchronous: 2 Mbps, 1 Mbps, 500 Kbps, and 250 Kbps
- Permits setting of any desired baud rate according to an external clock input
- Error detection function (parity errors, framing errors, and overrun errors)
- NRZ code as transfer signal
- Supports Intelligent I/O Service

(1) Register Configuration

Serial mode register 1
Address : channel 1 000024H

	7	6	5	4	3	2	1	0	←Bit no.
	MD1	MD0	CS2	CS1	CS0	BCH	SCKE	SOE	SMR
Read/write→	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Serial control register 1
Address : channel 1 000025H

	15	14	13	12	11	10	9	8	←Bit no.
	PEN	P	SBL	CL	A/D	REC	RXE	TXE	SCR
Read/write→	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(W)	(R/W)	(R/W)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(1)	(0)	(0)	

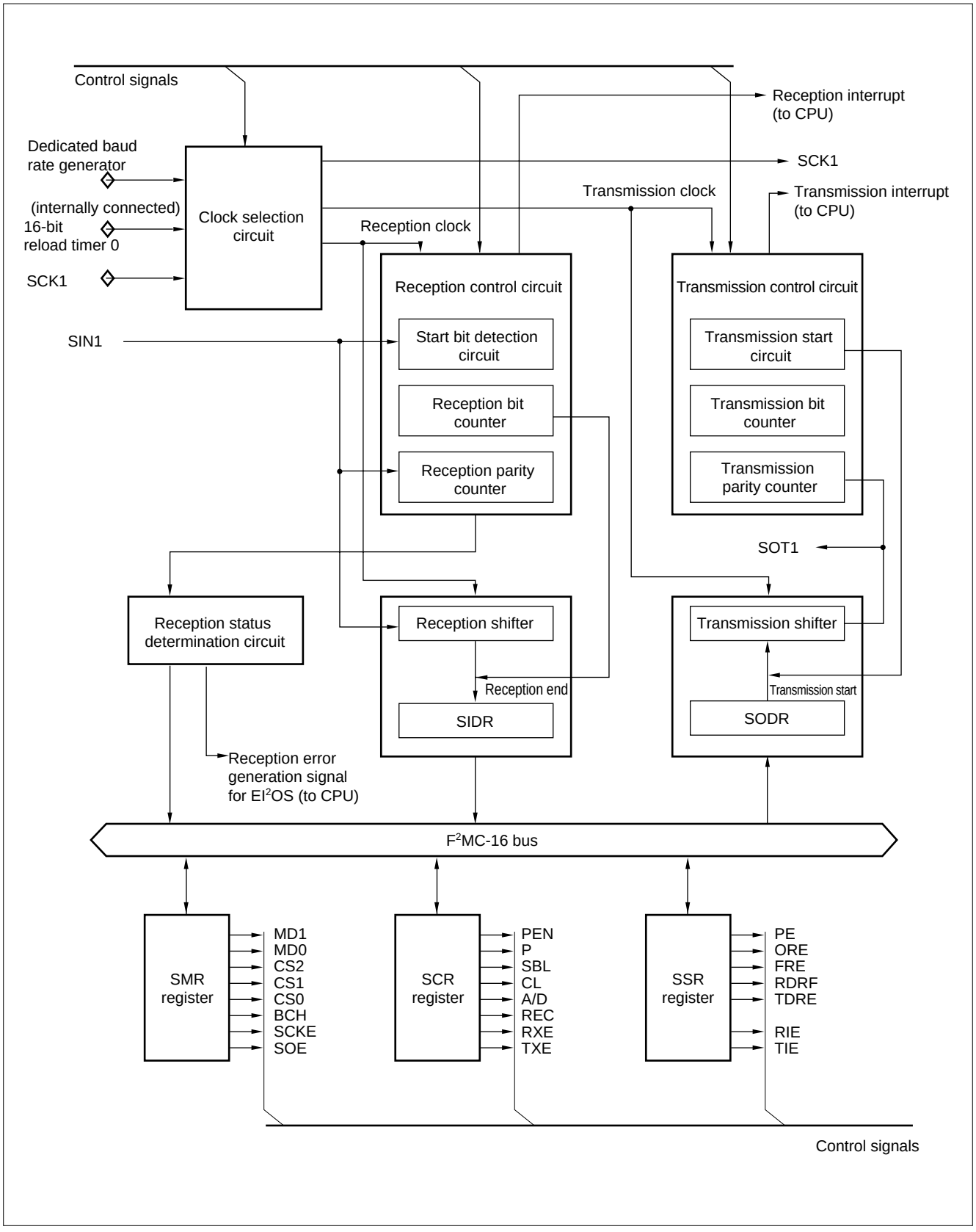
Serial input data register 1/
Serial output data register 1
Address : channel 1 000026H

	7	6	5	4	3	2	1	0	←Bit no.
	D7	D6	D5	D4	D3	D2	D1	D0	SIDR (read)/ SODR (write)
Read/write→	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value→	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

Serial status register 1
Address : channel 1 000027H

	15	14	13	12	11	10	9	8	←Bit no.
	PE	ORE	FRE	RDRF	TDRE	—	RIE	TIE	SSR
Read/write→	(R)	(R)	(R)	(R)	(R)	(—)	(R/W)	(R/W)	
Initial value→	(0)	(0)	(0)	(0)	(1)	(—)	(0)	(0)	

(2) Block Diagram



4. 10-bit 8-channel A/D Converter (with 8-bit Resolution Mode)

The 10-bit 8-channel A/D converter converts analog input voltage into a digital value. The features of this module are as follows:

- Conversion time: Minimum of 6.13 µs per channel (98 machine cycles/16 MHz machine clock, including sampling time)
- Sampling time: Minimum of 3.75 µs per channel (60 machine cycles/16 MHz machine clock)
- RC-type successive approximation conversion method with sample and hold circuit
- 10-bit/8-bit resolution
- Analog input is selectable by software from among 8 channels
  Single-conversion mode: Selects and converts one channel.
  Scan conversion mode: Converts several consecutive channels (up to eight channels can be programmed).
  Continuous conversion mode: Repeatedly converts the specified channel.
  Stop conversion mode: Pauses after converting one channel and waits until the next activation (permits synchronization of start of conversion).
- When A/D conversion is completed, an "A/D conversion complete" interrupt request can be issued to the CPU. Because generating this interrupt can be used to activate the I²OS and transfer the A/D conversion results to memory, this function is suitable for continuous processing.
- Activation sources can be selected from among software, an external trigger (falling edge), and 16-bit reload timer 1 (rising edge).

(1) Register Configuration

A/D converter control status register upper
Address : 00002D H

Bit no.	15	14	13	12	11	10	9	8	
	BUSY	INT	INTE	PAUS	STS1	STS0	STRT	Reserved	ADCS
Read/write→	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(W)	(—)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

A/D converter control status register lower
Address : 00002C H

Bit no.	7	6	5	4	3	2	1	0	
	MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0	ADCS
Read/write→	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

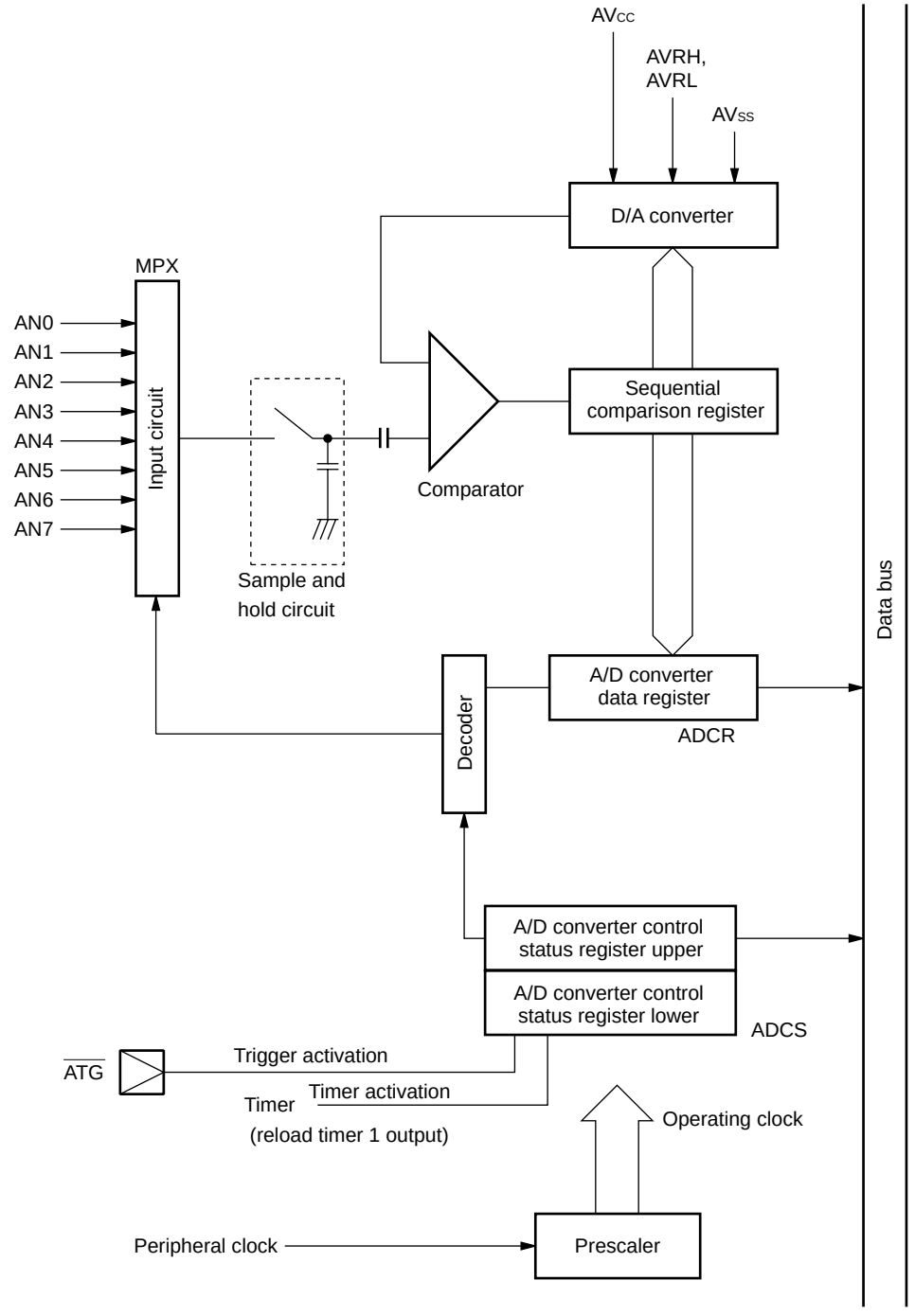
A/D converter data register upper
Address : 00002F H

Bit no.	15	14	13	12	11	10	9	8	
	S10	—	—	—	—	—	D9	D8	ADCR
Read/write→	(R/W)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(X)	(X)	

A/D converter data register lower
Address : 00002E H

Bit no.	7	6	5	4	3	2	1	0	
	D7	D6	D5	D4	D3	D2	D1	D0	ADCR
Read/write→	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value→	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

(2) Block Diagram



5. PPG

PPG is an 8-bit reload timer module that generates PPG output through pulse output control in accordance with the timer operation.

In terms of hardware, this module consists of two 8-bit down counters, four 8-bit PPG reload registers, one 16-bit PPG operating mode control register, two external pulse output pins, and two interrupt outputs. This hardware is used to implement the following functions:

- 8-bit PPG output two-channel independent operating mode: Permits independent PPG output operation on two channels.
- 16-bit PPG output operating mode: Permits PPG output operations on one 16-bit channel.
- 8 + 8-bit PPG output operating mode: Permits 8-bit PPG output operation with any cycle by using the channel 0 output as the channel 1 clock input.
- PPG output operation: Outputs a pulse waveform with any cycle and any duty ratio. Can also be used as a D/A converter by providing an external circuit.

(1) Register Configuration

PPG0 operating mode control register
Address : channel 0 000030H

Bit no.	7	6	5	4	3	2	1	0	
	PEN0	—	POE0	PIE0	PUF0	PCM1	PCM0	Reserved	PPGC0
Read/write →	(R/W)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(—)	
Initial value →	(0)	(—)	(0)	(0)	(0)	(0)	(0)	(1)	

PPG1 operating mode control register
Address : channel 1 000031H

Bit no.	15	14	13	12	11	10	9	8	
	PEN1	PCS1	POE1	PIE1	PUF1	MD1	MD0	Reserved	PPGC1
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(—)	
Initial value →	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(1)	

- PPG0 reload register upper
- PPG1 reload register upper

Address : channel 0 000035H
channel 1 000037H

Bit no.	15	14	13	12	11	10	9	8	
									PRLH0
									PRLH1
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

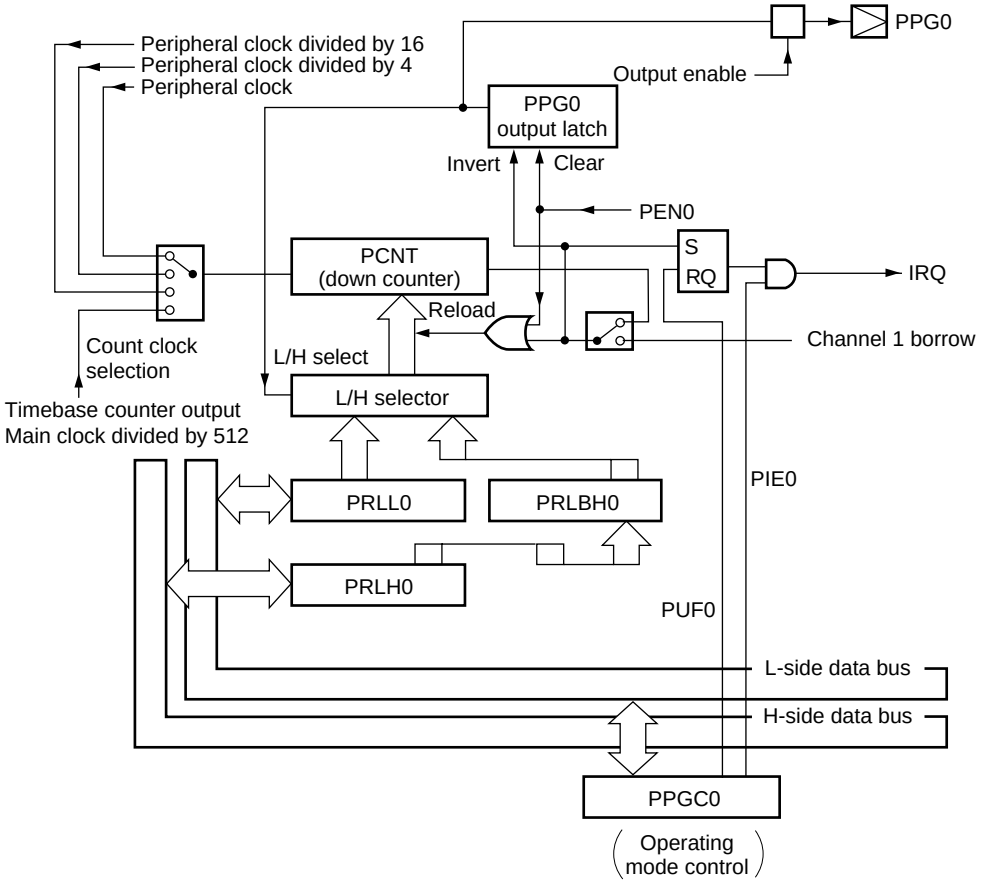
- PPG0 reload register lower
- PPG1 reload register lower

Address : channel 0 000034H
channel 1 000036H

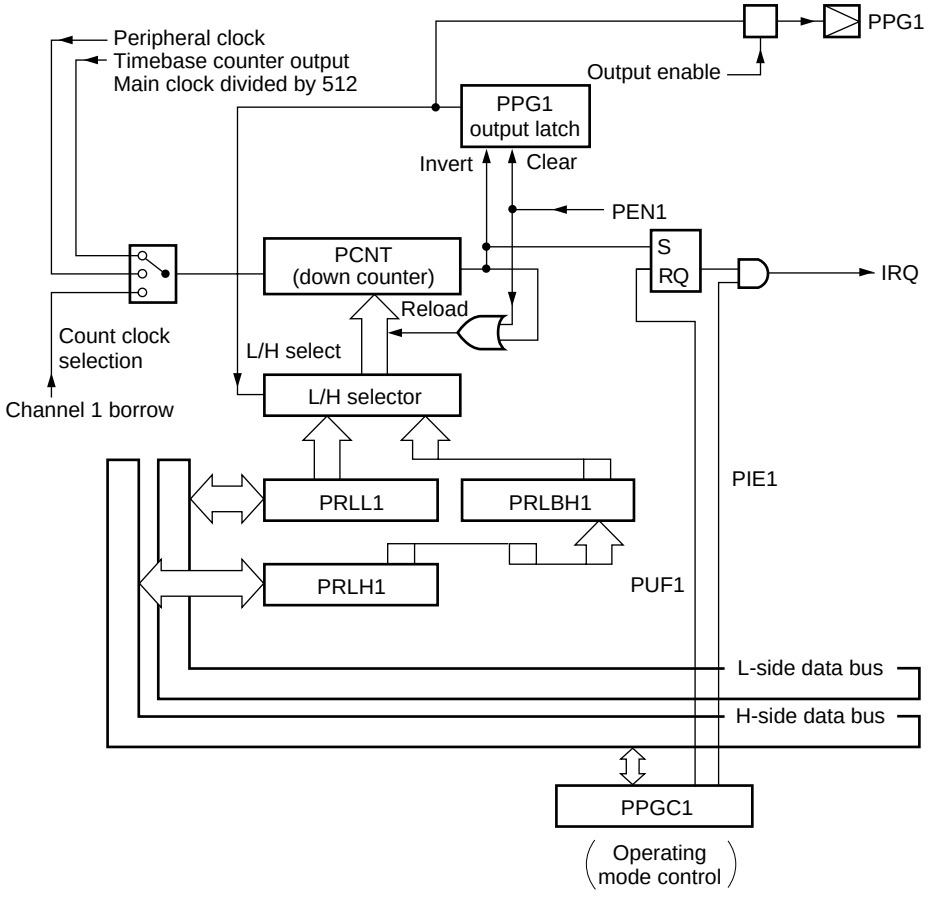
Bit no.	7	6	5	4	3	2	1	0	
									PRLL0
									PRLL1
Read/write →	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value →	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

(2) Block Diagram

• **Channel 0**



• **Channel 1**

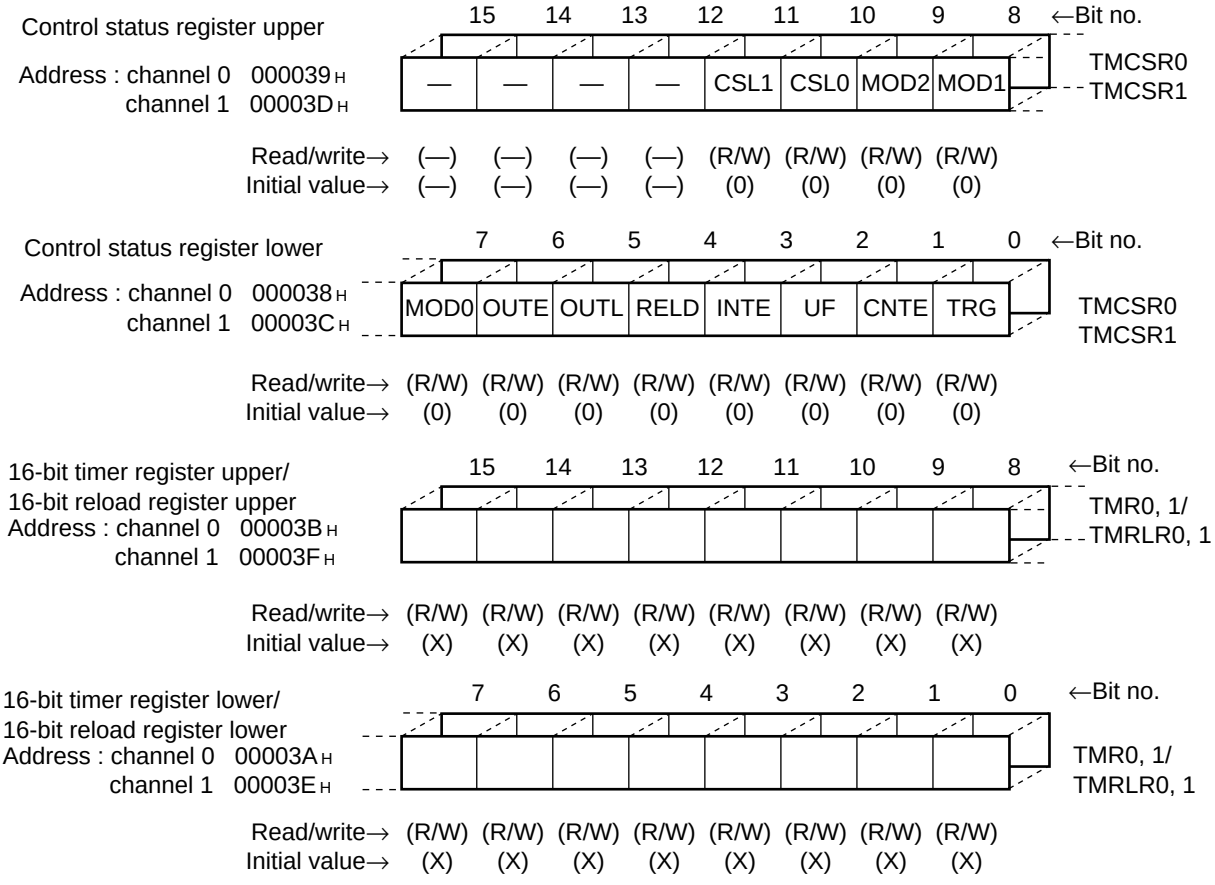

Peripheral clock
Timebase counter output
Main clock divided by 512
PPG1
Output enable
PPG1
output latch
Invert
Clear
PEN1
PCNT
(down counter)
S
RQ
IRQ
Reload
Count clock
selection
L/H select
Channel 1 borrow
L/H selector
PRLL1
PRLBH1
PIE1
PRLH1
PUF1
L-side data bus
H-side data bus
PPGC1
Operating
mode control

6. 16-bit Reload Timer (with Event Count Function)

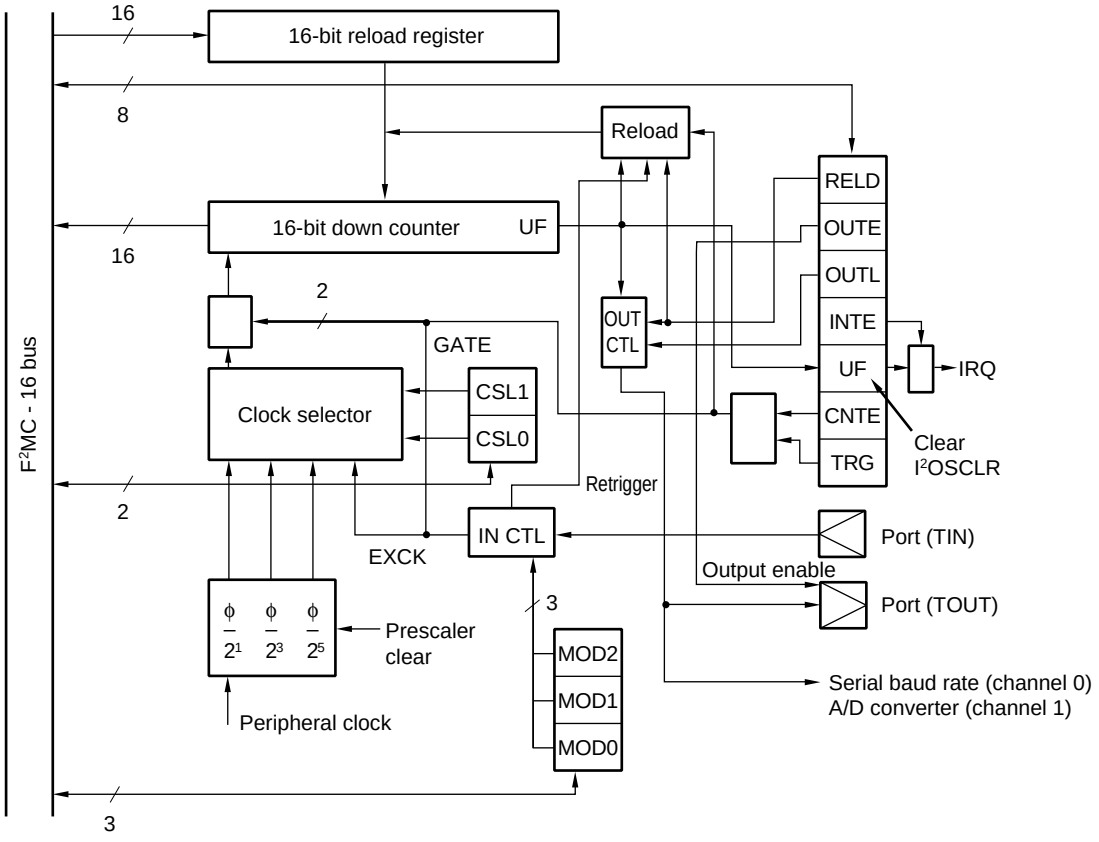
The 16-bit reload timer consists of a 16-bit down counter, a 16-bit reload register, one input pin (TIN), one output pin (TOUT), and a control status register. Three internal clocks and an external clock can be selected for the input clock. When in reload mode, a toggled output waveform is output, while in one-shot mode a square wave indicating that the count is in progress is output. The input pin (TIN) serves as an event input in event count mode, and can be used for trigger input or gate input in internal clock mode.

In this product, there are two channels for this timer on chip.

(1) Register Configuration



(2) Block Diagram



7. 24-bit Free-run Timer

The 24-bit free-run timer consists of a 24-bit up counter, an 8-bit output buffer, and a free-run timer control register. The counter value output from this free-run timer is used for basic time generation by the input capture and output compare units.

The interrupt functions are the timer overflow interrupt and timer intermediate bit interrupt; four different time settings can be made for the intermediate bit interrupt.

A reset clears the timer counter value for the 24-bit free-run timer to all zeroes.

(1) Register Configuration

Free-run timer control register upper
Address : 000051 H

	15	14	13	12	11	10	9	8	←Bit no.
	—	—	Reserved	Reserved	Reserved	Reserved	Reserved	PR0	TCCR
Read/write→	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	
Initial value→	(—)	(—)	(1)	(1)	(1)	(1)	(1)	(1)	

Free-run timer control register lower
Address : 000050 H

	7	6	5	4	3	2	1	0	←Bit no.
	STP	CLR	IVF	IVFE	TIM	TIME	TIS1	TIS0	TCCR
Read/write→	(W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value→	(1)	(1)	(0)	(0)	(0)	(0)	(0)	(0)	

Free-run timer lower
16-bit data register upper
Address : 000055 H

	15	14	13	12	11	10	9	8	←Bit no.
									TCRL
Read/write→	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Free run timer lower
16-bit data register lower
Address : 000054 H

	7	6	5	4	3	2	1	0	←Bit no.
									TCRL
Read/write→	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

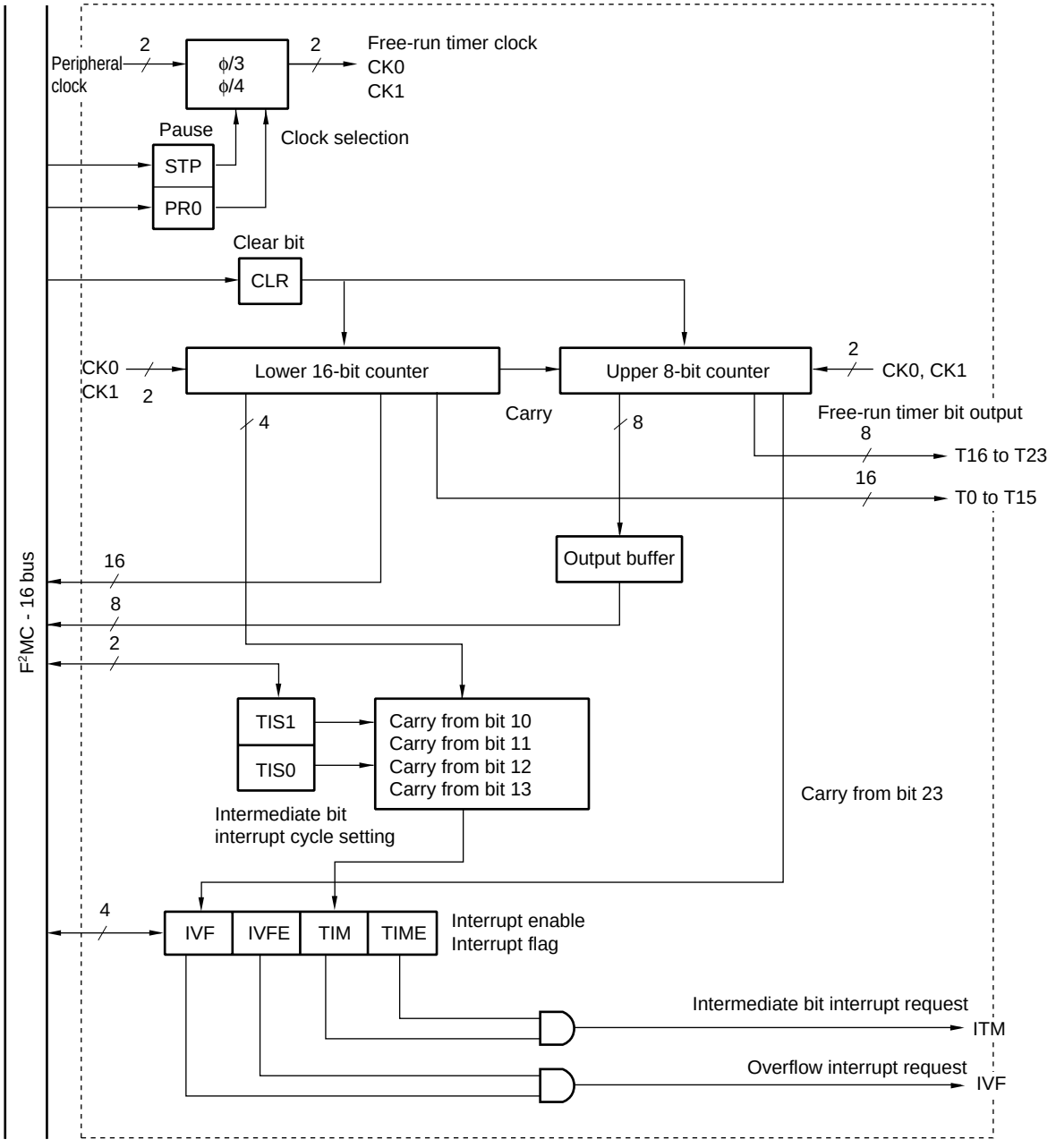
Free-run timer upper
8-bit data register upper
Address : 000057 H

	15	14	13	12	11	10	9	8	←Bit no.
									TCRH
Read/write→	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Free run timer upper
8-bit data register lower
Address : 000056 H

	7	6	5	4	3	2	1	0	←Bit no.
									TCRH
Read/write→	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

(2) Block Diagram



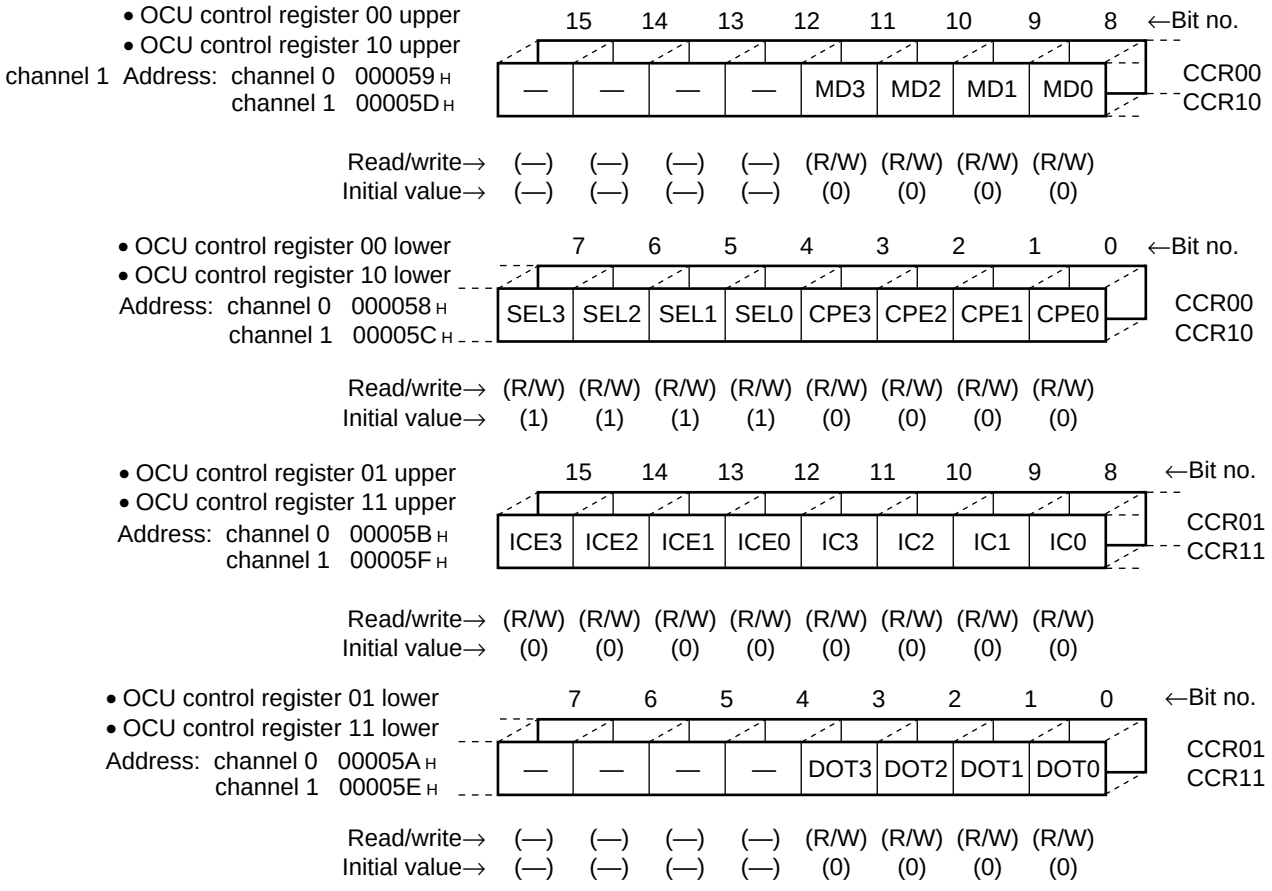
8. OCU (Output Compare)

The output compare unit consists of a 24-bit OCU register, a comparator, and an OCU control register. When the contents of the OCU register and the 24-bit timer counter match, the match detection signal is output. This match detection signal can be used to change the output values of the corresponding pins, or else to generate an interrupt. One output compare block consists of four channels, and time division comparisons can be made with one comparator for the four channels.

The compare precision of this OCU is four times the operation cycle of the 24-bit free-run timer; if the 24-bit free-run timer operates at 4 MHz, the compare precision is 1 µs.

The MB90670/675 series has two of these OCUs on chip.

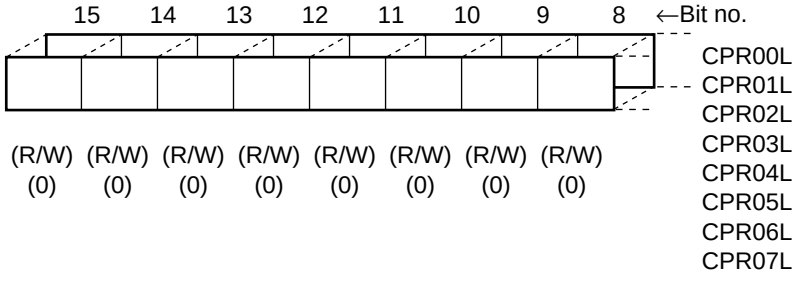
(1) Register Configuration



MB90670/675 Series

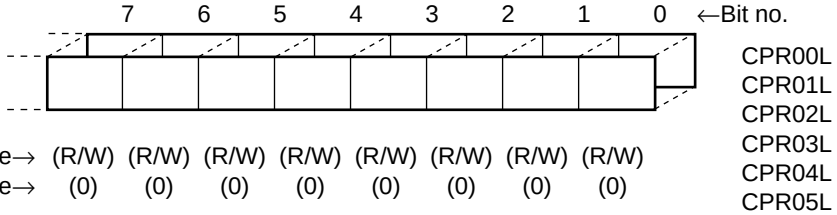
OCU compare lower data register upper

Address : channel 0 000071H
channel 1 000075H
channel 2 000079H
channel 3 00007DH
channel 4 000081H
channel 5 000085H
channel 6 000089H
channel 7 00008DH



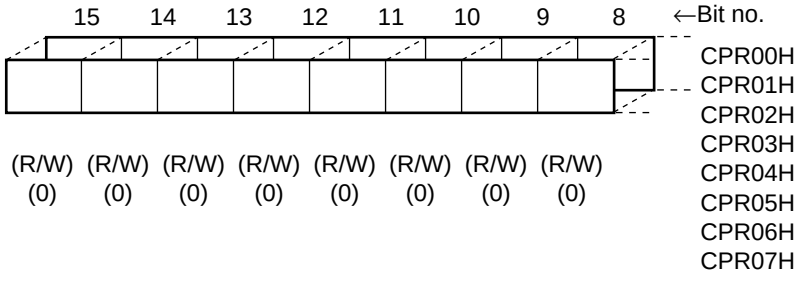
OCU compare lower data register lower

Address : channel 0 000070H
channel 1 000074H
channel 2 000078H
channel 3 00007CH
channel 4 000080H
channel 5 000084H
channel 6 000088H
channel 7 00008CH



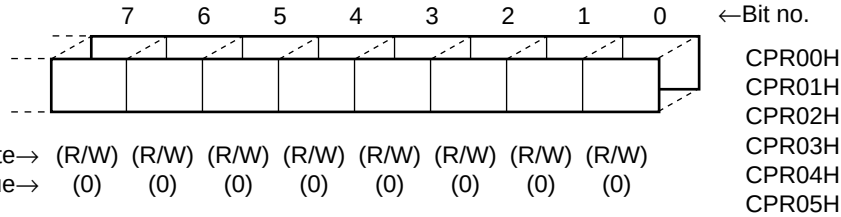
OCU compare upper data register upper

Address : channel 0 000073H
channel 1 000077H
channel 2 00007BH
channel 3 00007FH
channel 4 000083H
channel 5 000087H
channel 6 00008BH
channel 7 00008FH

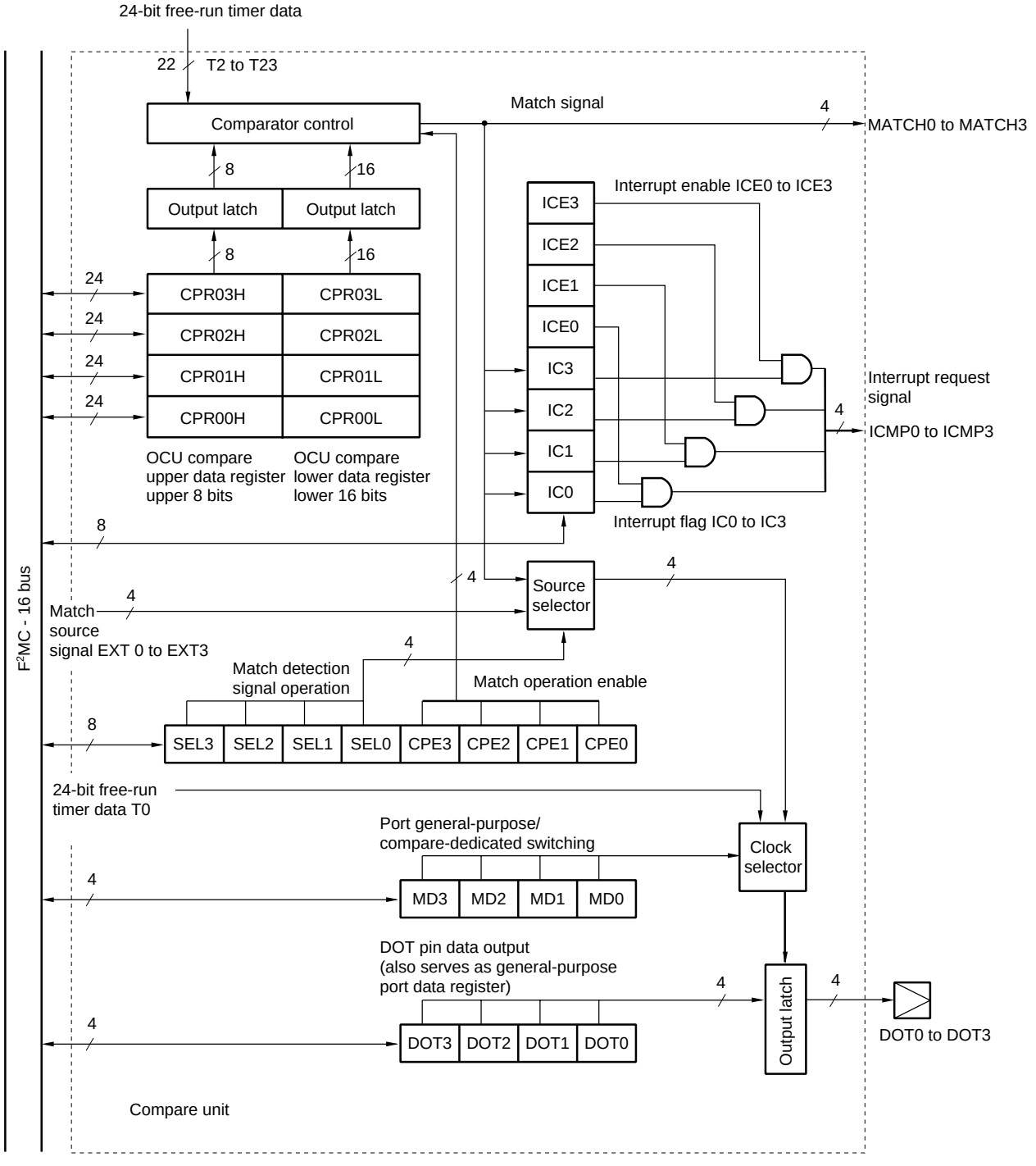


OCU compare upper data register lower

Address : channel 0 000072H
channel 1 000076H
channel 2 00007AH
channel 3 00007EH
channel 4 000082H
channel 5 000086H
channel 6 00008AH
channel 7 00008EH

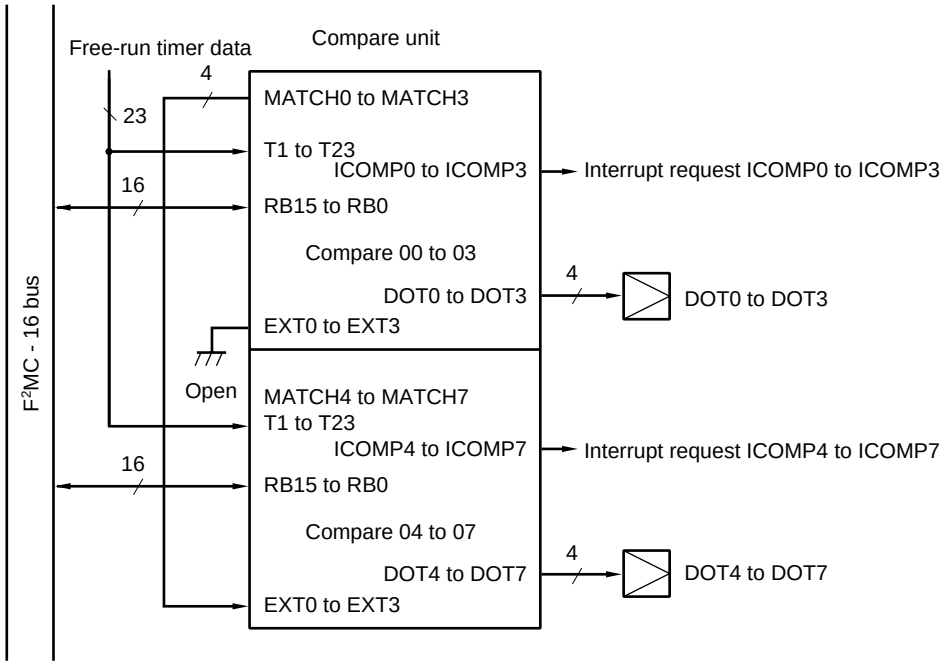


(2) Block Diagram



Note: There are two complete compare units.

(3) Overall Configuration



9. ICU (Input Capture)

ICU detects the rising edge, falling edge, or both edges of an externally input waveform and then saves the counter value of the 24-bit free-run timer, while simultaneously generating an interrupt request for the CPU. The module hardware consists of four 24-bit ICU data registers and an ICU control register. There are four external input pins (AS0 to AS3), and each pin is used to implement the operation indicated below.

The capture precision of this ICU is equal to the operation cycle of the 24-bit free-run timer; if the 24-bit free-run timer operates at 4 MHz, the capture precision is 250 ns.

- AS0 to AS3: These input pins each have one ICU register; the counter value of the 24-bit free-run timer can be retained when the specified valid edge (↑, ↓, or ↑ ↓) is generated.

(1) Register Configuration

ICU control register upper

Address : 000053 H

Bit no.	15	14	13	12	11	10	9	8	
	IRE3	IRE2	IRE1	IRE0	IR3	IR2	IR1	IR0	ICC
Read/write→	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

ICU control register lower

Address : 000052 H

Bit no.	7	6	5	4	3	2	1	0	
	EG3B	EG3A	EG2B	EG2A	EG1B	EG1A	EG0B	EG0A	ICC
Read/write→	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

ICU lower data register upper

Address : channel 0 000061 H
channel 1 000065 H
channel 2 000069 H
channel 3 00006D H

Bit no.	15	14	13	12	11	10	9	8	
									ICR0L
									ICR1L
									ICR2L
									ICR3L
Read/write→	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value→	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

ICU lower data register lower

Address : channel 0 000060 H
channel 1 000064 H
channel 2 000068 H
channel 3 00006C H

Bit no.	7	6	5	4	3	2	1	0	
									ICR0L
									ICR1L
									ICR2L
									ICR3L
Read/write→	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value→	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

ICU upper data register upper

Address : channel 0 000063 H
channel 1 000067 H
channel 2 00006B H
channel 3 00006F H

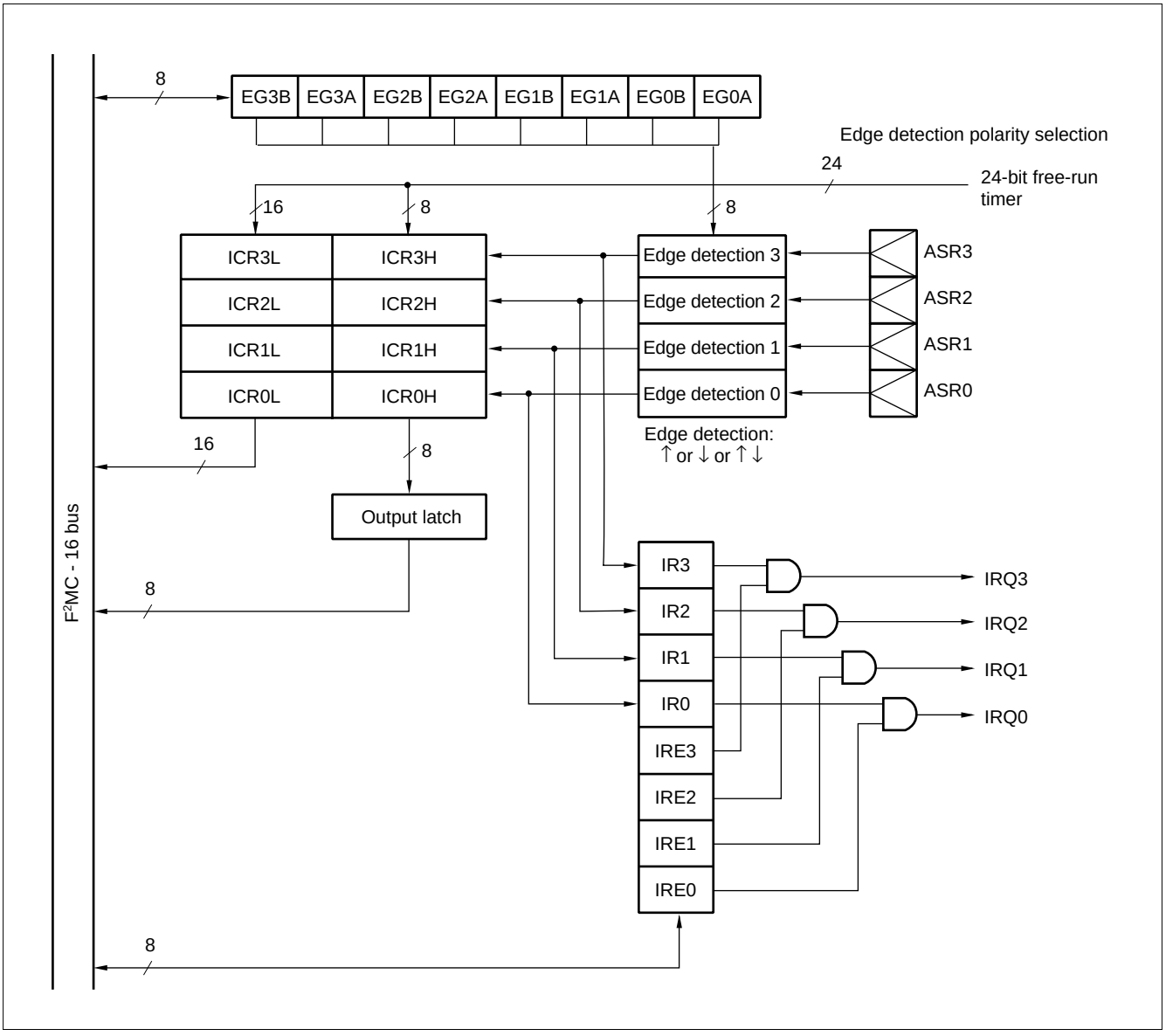
Bit no.	15	14	13	12	11	10	9	8	
									ICR0H
									ICR1H
									ICR2H
									ICR3H
Read/write→	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

ICU upper data register upper

Address : channel 0 000062 H
channel 1 000066 H
channel 2 00006A H
channel 3 00006E H

Bit no.	7	6	5	4	3	2	1	0	
									ICR0H
									ICR1H
									ICR2H
									ICR3H
Read/write→	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value→	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

(2) Block Diagram



10. DTP/External Interrupt

The DTP (Data Transfer Peripheral) is a peripheral, positioned between peripherals external to the device and the F²MC-16L CPU, that accepts DMA requests or interrupt requests generated by external peripherals and transfers them to the F²MC-16L CPU to activate the Intelligent I/O Service or interrupt processing. In the case of the Intelligent I/O Service, there are two request levels that can be selected: high and low; in the case of an external interrupt request, there are a total of four request levels that can be selected: high, low, rising edge and falling edge.

(1) Register Configuration

Interrupt/DTP enable register — Address : 000028 H — ENIR

Bit no.	7	6	5	4	3	2	1	0
	—	—	—	—	EN3	EN2	EN1	EN0
Read/write→	(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value→	(—)	(—)	(—)	(—)	(0)	(0)	(0)	(0)

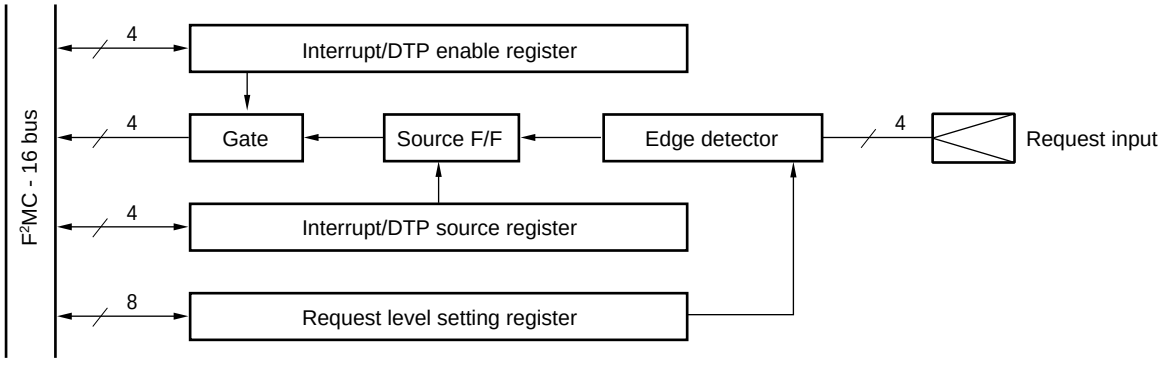
Interrupt/DTP source register — Address : 000029 H — EIRR

Bit no.	15	14	13	12	11	10	9	8
	—	—	—	—	ER3	ER2	ER1	ER0
Read/write→	(—)	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value→	(—)	(—)	(—)	(—)	(0)	(0)	(0)	(0)

Request level setting register — Address : 00002A H — ELVR

Bit no.	7	6	5	4	3	2	1	0
	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0
Read/write→	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

(2) Block Diagram



11. Wake-up Interrupt

The wake-up interrupt is a peripheral, positioned between peripherals external to the device and F²MC-16L CPU. This interrupt accepts interrupt requests generated by external peripherals and transfers them to the F²MC-16L CPU to acvitate interrupt processing.

An interrupt request is generated by input signal of “L” level.

(1) Register Configuration

Wake-up interrupt enable register

Address : 00001F H

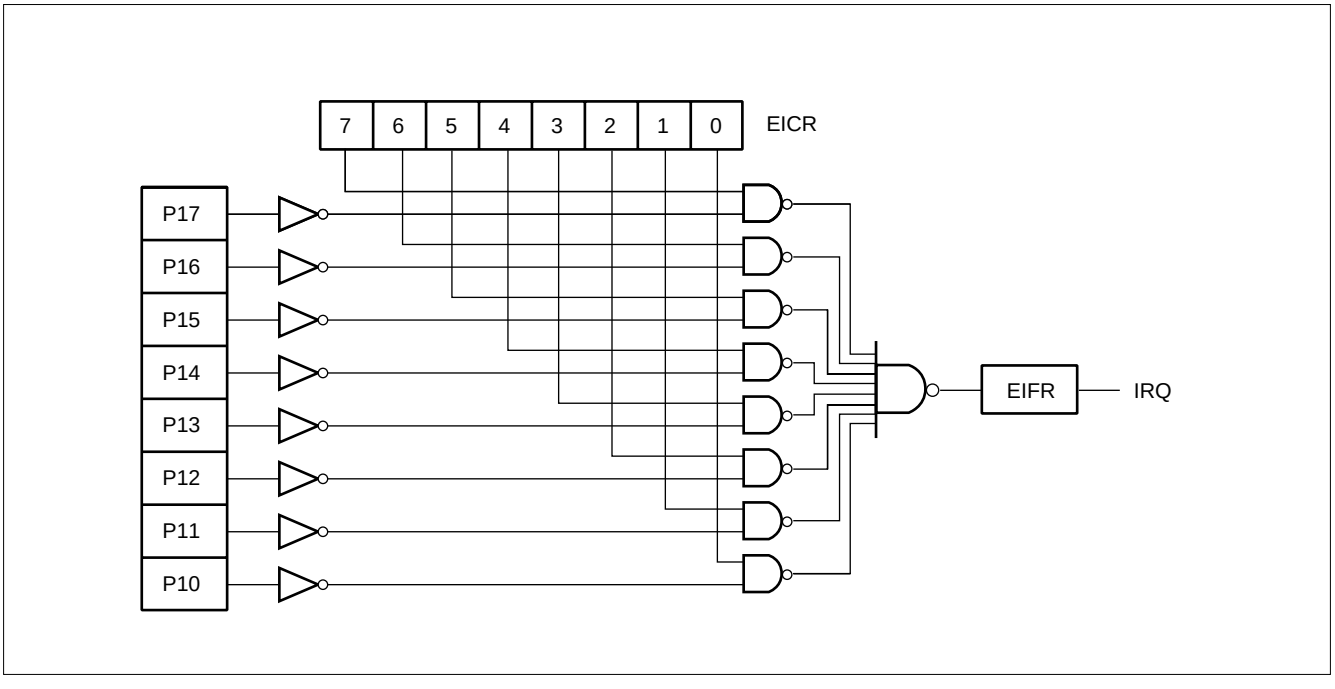
	15	14	13	12	11	10	9	8	←Bit no.
	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	EICR
Read/write→	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Wake-up interrupt flag register

Address : 00000F H

	15	14	13	12	11	10	9	8	←Bit no.
	—	—	—	—	—	—	—	WIF	EIFR
Read/write→	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	
Initial value→	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)	

(2) Block Diagram



12. Delayed Interrupt Generation Module

The delayed interrupt generation module generates task switching interrupts. This module can be used to generate/cancel interrupt requests to the F²MC-16L CPU by software.

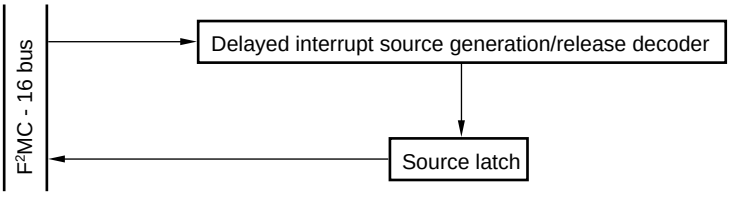
(1) Register Configuration

Delayed interrupt source generation/release register

Address : 00009F H

	15	14	13	12	11	10	9	8	←Bit no.
	—	—	—	—	—	—	—	R0	DIRR
Read/write→	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	
Initial value→	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)	

(2) Block Diagram



13. I²C Interface

The I²C interface is a serial I/O port that supports the Inter-IC bus and operates as a master/slave device on the I²C bus. This module has the following features:

- Master slave transmission/reception
- Arbitration function
- Clock synchronization function
- Slave address/general call address detection function
- Transfer direction detection function
- Start condition repeat generation ad detection function
- Bus error detection function

The MB90675 series is provided with a single channel of this module.
This module has one channel on chip in the MB90675 series.

(1) Register Configuration

I²C bus status register
Address : 000040H

Bit no.	7	6	5	4	3	2	1	0	
	BB	RSC	AL	LRB	TRX	AAS	GCA	FBT	IBSR
Read/write→	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

I²C bus control register
Address : 000041H

Bit no.	15	14	13	12	11	10	9	8	
	BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT	IBCR
Read/write→	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value→	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

I²C bus clock selection register
Address : 000042H

Bit no.	7	6	5	4	3	2	1	0	
	—	—	EN	CS4	CS3	CS2	CS1	CS0	ICCR
Read/write→	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value→	(—)	(—)	(0)	(X)	(X)	(X)	(X)	(X)	

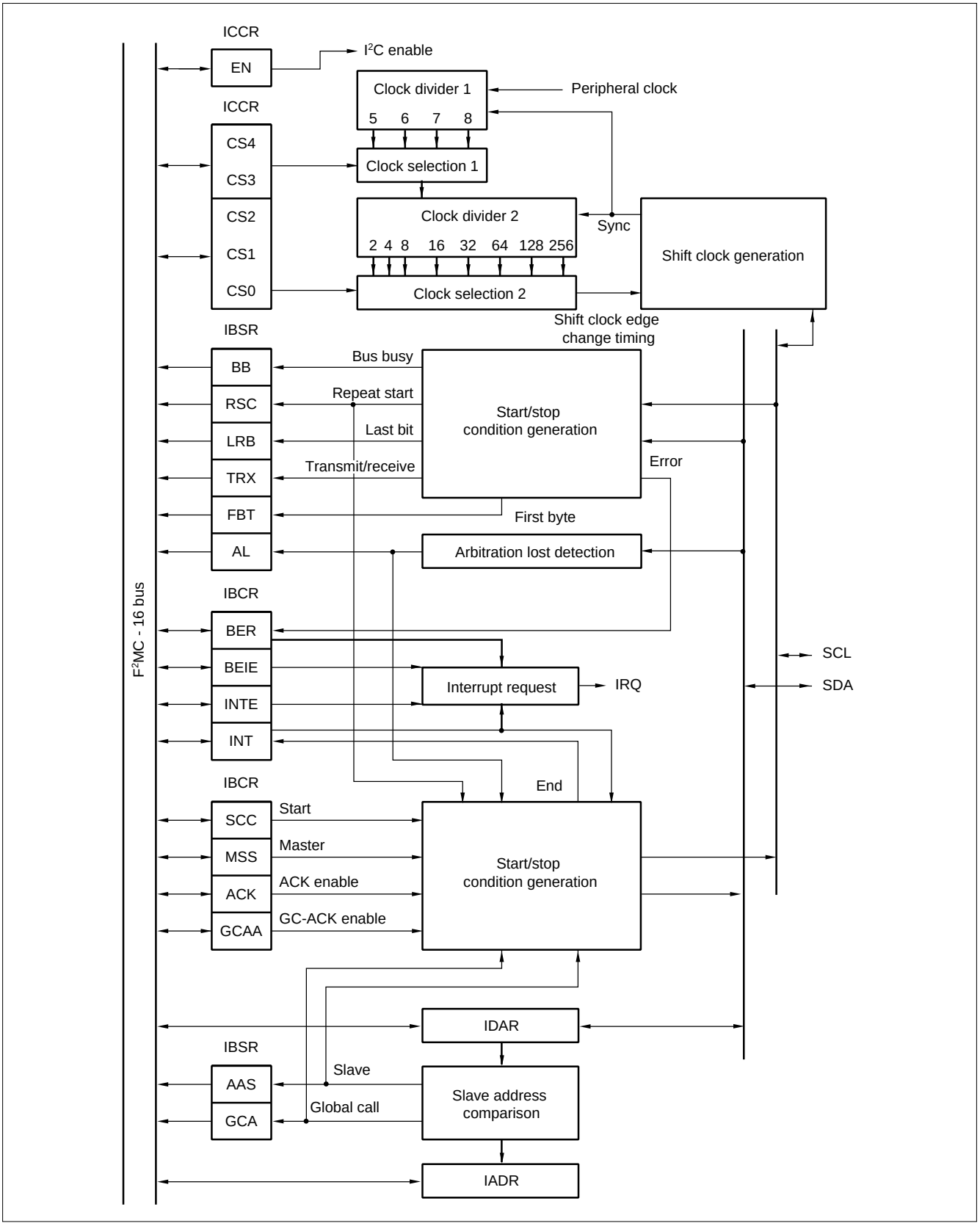
I²C bus address register
Address : 000043H

Bit no.	15	14	13	12	11	10	9	8	
	—	A6	A5	A4	A3	A2	A1	A0	IADR
Read/write→	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value→	(—)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

I²C bus data register
Address : 000044H

Bit no.	7	6	5	4	3	2	1	0	
	D7	D6	D5	D4	D3	D2	D1	D0	IDAR
Read/write→	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial value→	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

(2) Block Diagram



14. Watchdog Timer and Timebase Timer Functions

The watchdog timer consists of a 2-bit watchdog counter that uses the carry signal from the 18-bit timebase timer as a clock source, a watchdog timer control register, and a watchdog reset controller.

The timebase timer consists of an 18-bit timer and a circuit that controls interval interrupts. Note that the time-base timer uses the main clock, regardless of the setting of the MCS bit in CKSCR.

(1) Register Configuration

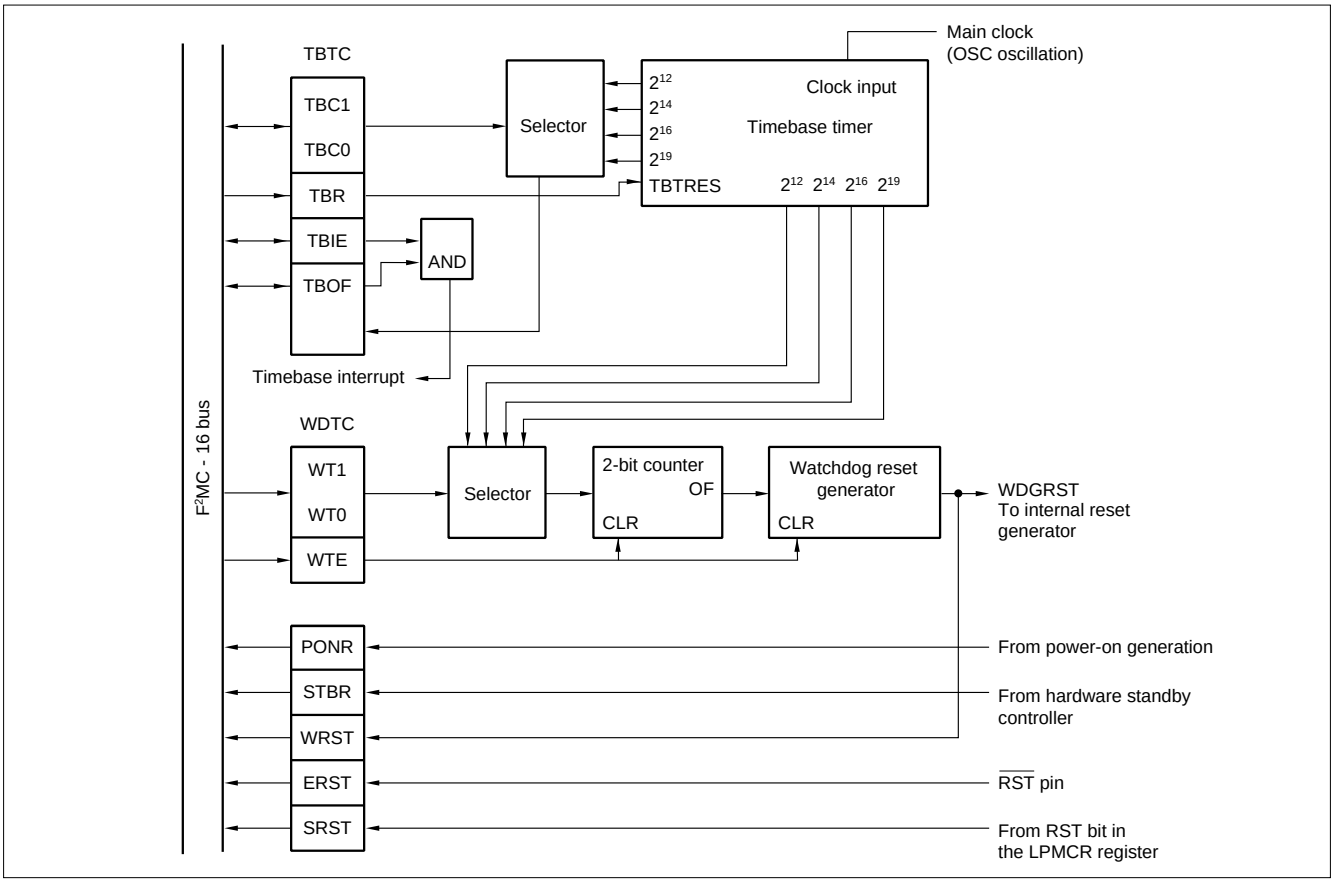
Watchdog timer control register

	7	6	5	4	3	2	1	0	←Bit no.
Address : 0000A8 H	PONR	STBR	WRST	ERST	SRST	WTE	WT1	WT0	WDTC
Read/write→	(R)	(R)	(R)	(R)	(R)	(W)	(W)	(W)	
Initial value→	(X)	(X)	(X)	(X)	(X)	(1)	(1)	(1)	

Timebase timer control register

	15	14	13	12	11	10	9	8	←Bit no.
Address : 0000A9 H	Reserved	—	—	TBIE	TBOF	TBR	TBC1	TBC0	TBTC
Read/write→	(—)	(—)	(—)	(R/W)	(R/W)	(W)	(R/W)	(R/W)	
Initial value→	(1)	(—)	(—)	(0)	(0)	(1)	(0)	(0)	

(2) Block Diagram



15. Low-power Consumption Controller (CPU Intermittent Operation Function, Oscillation Stabilization Delay Time, Clock Multiplier Function)

The following are the operating modes: PLL clock mode, PLL sleep mode, watch mode, main clock mode, main sleep mode, stop mode, and hardware standby mode. Aside from the PLL clock mode, all of the other operating modes are low power consumption modes.

In main clock mode and main sleep mode, only the main clock (main OSC oscillation clock) operates. In these modes, the main clock divided by 2 is used as the operation clock, and the PLL clock (VCO oscillation clock) is stopped.

In PLL sleep mode and main sleep mode, only the CPU's operation clock is stopped; all clocks other than the CPU clock operate.

In watch mode, only the time-base timer operates.

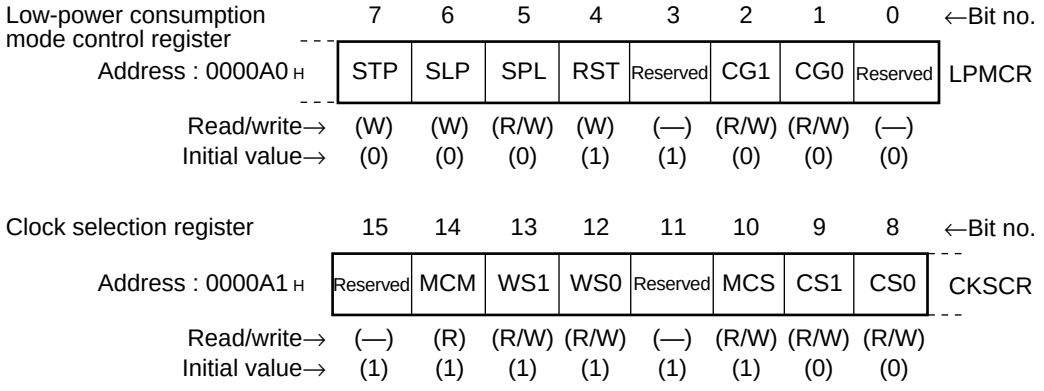
The stop mode and hardware standby mode stop oscillation, making it possible to retain data while consuming the least amount of power .

The CPU intermittent operation function intermittently runs the clock supplied to the CPU when accessing registers, on-chip memory, on-chip resources, and the external bus. Processing is possible with lower power consumption by reducing the execution speed of the CPU while supplying a high-speed clock and using on-chip resources.

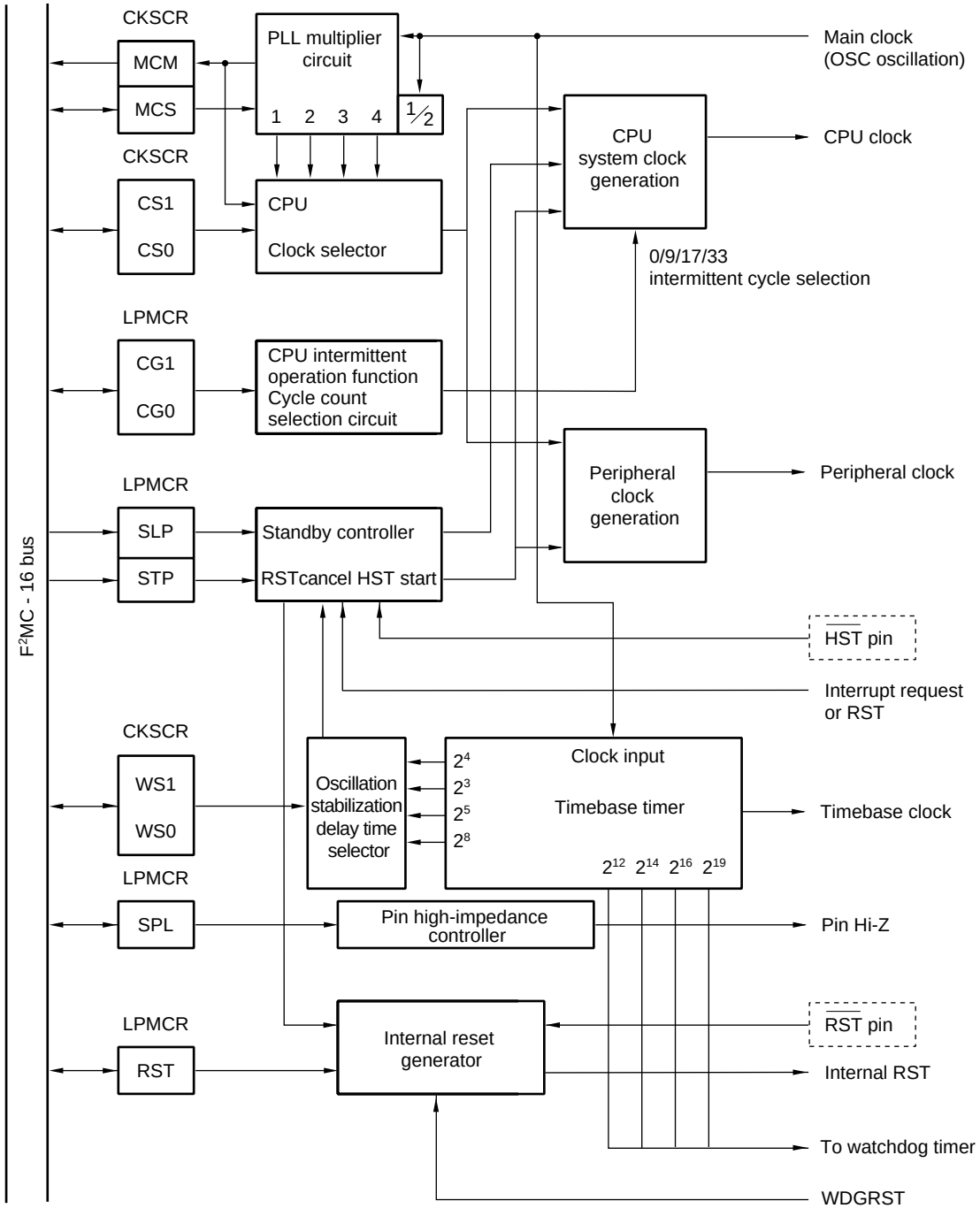
The PLL clock multiplier can be selected as either 1, 2, 3, or 4 by setting the CS1 and CS0 bits.

The WS1 and WS0 bits can be used to set the main clock oscillation stabilization delay time for when stop mode and hardware standby mode are woken up.

(1) Register Configuration



(2) Block Diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
	AV_{CC}	V_{CC} – 0.3	V_{CC} + 7.0	V	*1
	AVRH AVRL	V_{CC} – 0.3	V_{CC} + 7.0	V	
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	*2
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	*2
“L” level maximum output current	I_{OL}	—	15	mA	*3
“L” level average output current	I_{OLAV}	—	4	mA	*4
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	*5
“H” level maximum output current	I_{OH}	—	–15	mA	*3
“H” level average output current	I_{OHAV}	—	–4	mA	*4
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–50	mA	*5
Power consumption	P_D	—	+400	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{stg}	–55	+150	°C	

*1: AV_{CC}, AVRH and AVRL must not exceed V_{CC}. In addition, AVRL must not exceed AVRH.
*2: V_I and V_O must not exceed V_{CC} + 0.3 V.
*3: The maximum output current defines the peak value on one of the pins in question.
*4: The average output current defines the average current over a 100 ms period for the current flowing to one of the pins in question.
*5: The total average output current defines the average current over a 100 ms period for the current flowing to all of the pins in question.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.7	5.5	V	Normal operation
		2.0	5.5	V	Maintaining the stop status
"H" level input voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	Pins other than V_{IHS} and V_{IHM}
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	Hysteresis input pins*
	V_{IHM}	V_{CC} – 0.3	V_{CC} + 0.3	V	MD pin input
"L" level input voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	Pins other than V_{ILS} and V_{ILM}
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	Hysteresis input pins*
	V_{ILM}	V_{SS} – 0.3	V_{CC} + 0.3	V	MD pin input
Operating temperature	T_A	–40	+85	°C	

* : The hysteresis input pins in the MB90670 series are: P24 to P27, P40 to P47, P60 to P67, P70 to P77, P80, $\overline{HST}$, and $\overline{RST}$.
The hysteresis input pins in the MB90675 series are: P24 to P27, P40 to P47, P60 to P67, P70 to P77, P80 to P86, $\overline{HST}$, $\overline{RST}$, P90, P91, PA0 to PA7, and PB0 to PB2.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

3. DC Characteristics

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level output voltage	V_{OH}	Other than P50 to P57	V_{CC} = +4.5 V I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
			V_{CC} = +2.7 V I_{OH} = –1.6 mA	V_{CC} – 0.3	—	—	V	
"L" level output voltage	V_{OL}	All output pins	V_{CC} = +4.5 V I_{OL} = 4.0 mA	—	—	0.4	V	
			V_{CC} = +2.7 V I_{OL} = 2.0 mA	—	—	0.4	V	
Input leakage current	I_{IL}	Other than P50 to P57, P90 and P91	V_{CC} = +5.0 V $V_{SS} < V_I < V_{CC}$	–10	—	10	µA	
Power supply current	I_{CC}	—	Internal 16 MHz operation V_{CC} = +5.0 V Normal operation*1	—	50	70	mA	
	I_{CCS}		Internal 16 MHz operation V_{CC} = +5.0 V Sleep mode*1	—	15	30	mA	
	I_{CC}	—	Internal 8 MHz operation V_{CC} = +3.0 V Normal operation*1	—	10	20	mA	
	I_{CCS}		Internal 8 MHz operation V_{CC} = +3.0 V Sleep mode*1	—	3	10	mA	
	I_{CCH}	—	T_A = +25°C Stop mode and hardware standby mode*1	—	0.1	10	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS} V_{CC}, V_{SS}	—	—	10	—	pF	
Open-drain output leakage current	I_{leak}	P50 to P57 P90, P91*2	—	—	0.1	10	µA	
Pull-up resistance	R	—	V_{CC} = +5.0 V	25	50	100	kΩ	
			V_{CC} = +3.0 V	40	100	200	kΩ	
Pull-down resistance	R	—	V_{CC} = +5.0 V	25	50	200	kΩ	
			V_{CC} = +3.0 V	40	100	400	kΩ	

*1: Because the current values are tentative values, they are subject to change without notice due to our efforts to improve the characteristics of these devices.

*2: P90 and P91 are provided only in the MB90675 series.

4. AC Characteristics

(1) Clock Timing

• When V_{CC} = +5.0 V ±10%

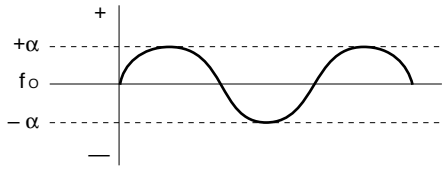
(V_{CC} = +4.5 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Source oscillation frequency	F_C	X0, X1	—	3	32	MHz	
Source oscillation cycle time	t_C	X0, X1	—	31.25	333	ns	
Input clock pulse width	P_{WH} P_{WL}	X0	—	10	—	ns	Use duty ratio 30 to 70% as a guide.
Input clock rising/falling time	t_{CR} t_{CF}	X0	—	—	5	ns	
Internal operation clock frequency	f_{CP}	—	—	1.5	16	MHz	
Internal operation clock cycle time	t_{CP}	—	—	62.5	666	ns	
When frequency fluctuation is locked	Δf	P37/CLK	—	—	3	%	*

* : The frequency fluctuation ratio indicates the maximum fluctuation ratio from the set center frequency while locked when using the PLL multiplier.

$$\Delta f = \frac{|\alpha|}{f_O} \times 100\ (\%)$$

Center frequency



Because the PLL frequency fluctuates around the set frequency with a certain cycle [approximately CLK × (1 to 50 CYC)], the worst value is not maintained for long. (The pulse, if featured with the long period, would produce practically no error.)

• When V_{CC} = +2.7 V (min.)

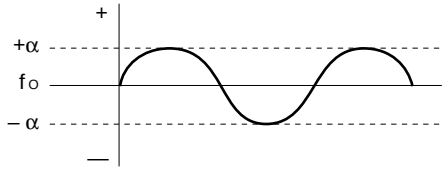
(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Source oscillation frequency	F_C	X0, X1	—	3	16	MHz	
Source oscillation cycle time	t_C	X0, X1	—	62.5	333	ns	
Input clock pulse width	P_{WH} P_{WL}	X0	—	20	—	ns	Use duty ratio 30 to 70% as a guide.
Input clock rising/falling time	t_{CR} t_{CF}	X0	—	—	5	ns	
Internal operation clock frequency	f_{CP}	—	—	1.5	8	MHz	
Internal operation clock cycle time	t_{CP}	—	—	125	666	ns	
When frequency fluctuation ratio is locked	Δf	P37/CLK	—	—	3	%	*

* : The frequency fluctuation ratio indicates the maximum fluctuation ratio from the set center frequency while locked when using the PLL multiplier.

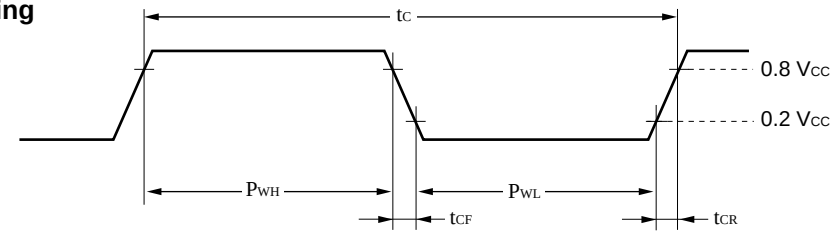
$$\Delta f = \frac{|\alpha|}{f_O} \times 100\ (\%)$$

Center frequency



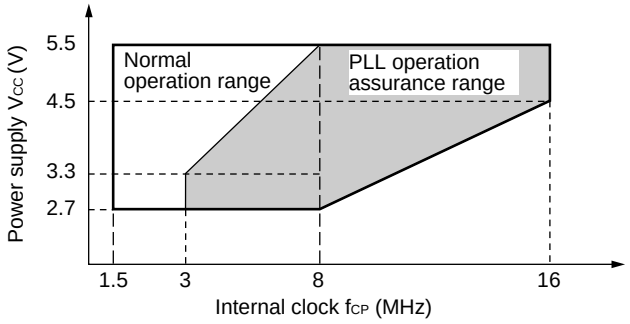
Because the PLL frequency fluctuates around the set frequency with a certain cycle [approximately CLK × (1 to 50 CYC)], the worst value is not maintained for long. (The pulse, if featured with the long period, would produce practically no error.)

- **Clock Timing**

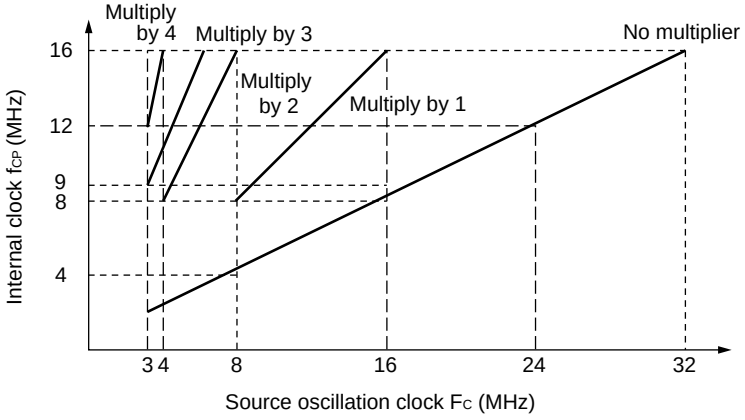


- **PLL Operation Assurance Range**

Relationship between internal operation clock frequency and power supply voltage



Relationship between source oscillation frequency, internal operating clock frequency, and power supply voltage

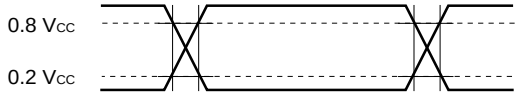


Note: Operation of the evaluation tool is also assured to +2.7 V on the low-voltage side.

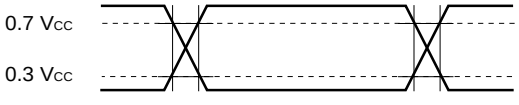
The AC characteristics are stipulated according to the measured reference voltages shown below.

- **Input Signal Waveform**

Hysteresis input pins

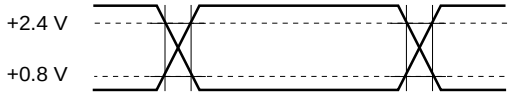


Other than hysteresis input/MD input pins



- **Output Signal Waveform**

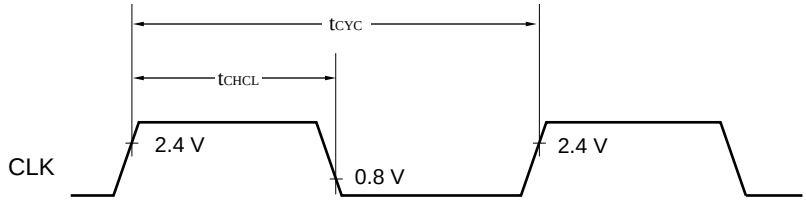
Output pin



(2) Clock Output Timing

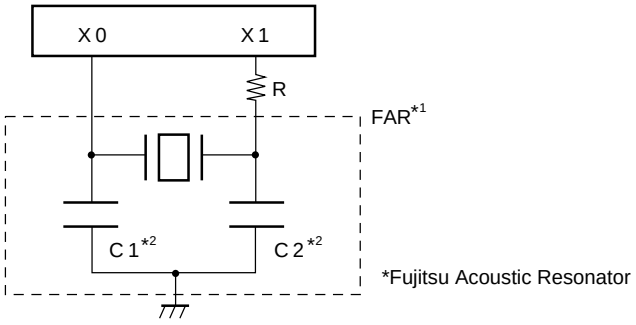
(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	t_{CP}	—	ns	
CLK ↑ → CLK↓	t_{CHCL}	CLK	—	$t_{CP}/2 - 20$	$t_{CP}/2 + 20$	ns	



(3) Recommended Resonator Manufacturers

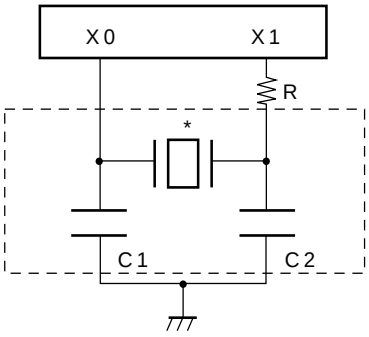
- **Sample Application of Piezoelectric Resonator (FAR Family)**



FAR part number (built-in capacitor type)	Frequency (MHz)	Dumping resistor	Initial deviation of FAR frequency (T_A = +25°C)	Temperature characteristics of FAR frequency (T_A = –20°C to +60°C)	Loading capacitors*2
FAR-C4□C-02000-□20	2.00	5.10 Ω	±0.5%	±0.5%	Built-in
FAR-C4□A-04000-□01	4.00	—	±0.5%	±0.5%	
FAR-C4□B-04000-□02			±0.5%	±0.5%	
FAR-C4□B-04000-□00			±0.5%	±0.5%	
FAR-C4□B-08000-□02	8.00	—	±0.5%	±0.5%	
FAR-C4□B-12000-□02	12.00	—	±0.5%	±0.5%	
FAR-C4□B-16000-□02	16.00	—	±0.5%	±0.5%	

Inquiry: FUJITSU LIMITED

- **Sample Application of Ceramic Resonator**



- **Mask Product**

Resonator manufacturer *	Resonator	Frequency (MHz)	C1 (pF)	C2 (pF)	R
Kyocera Corporation	KBR-2. 0MS	2.00	150	150	Not required
	PBRC2. 00A		150	150	Not required
	KBR-4. 0MSA	4.00	33	33	680 Ω
	KBR-4. 0MKS		Built-in	Built-in	680 Ω
	PBRC4. 00A		33	33	680 Ω
	PBRC4. 00B		Built-in	Built-in	680 Ω
	KBR-6. 0 MSA	6.00	33	33	Not required
	KBR-6. 0MKS		Built-in	Built-in	Not required
	PBRC6. 00A		33	33	Not required
	PBRC6. 00B		Built-in	Built-in	Not required
	KBR-8. 0M	8.00	33	33	560 Ω
	PBRC8. 00A		33	33	Not required
	PBRC8. 00B		Built-in	Built-in	Not required
	KBR-10. 0M	10.00	33	33	330 Ω
	PBRC10. 00B		Built-in	Built-in	680 Ω
	KBR-12. 0M	12.00	33	33	330 Ω
	PBRC12. 00B		Built-in	Built-in	680 Ω
Murata Mfg, Co., Ltd.	CSA2. 00MG040	2.00	100	100	Not required
	CST2. 00MG040		Built-in	Built-in	Not required
	CSA4. 00MG040	4.00	100	100	Not required
	CST4. 00MGW040		Built-in	Built-in	Not required
	CSA6. 00MG	6.00	30	30	Not required
	CST6. 00MGW		Built-in	Built-in	Not required
	CSA8. 00MTZ	8.00	30	30	Not required
	CST8. 00MTW		Built-in	Built-in	Not required
	CSA10. 0MTZ	10.00	30	30	Not required
	CST10. 0MTW		Built-in	Built-in	Not required
	CSA12. 0MTZ	12.00	30	30	Not required
	CST12. 0MTW		Built-in	Built-in	Not required

(Continued)

MB90670/675 Series

(Continued)

Resonator manufacturer *	Resonator	Frequency (MHz)	C1 (pF)	C2 (pF)	R
Murata Mfg, Co., Ltd.	CSA16. 00MXZ040	16.00	15	15	Not required
	CST16. 00MXW0C3		Built-in	Built-in	Not required
	CSA20. 00MXZ040	20.00	10	10	Not required
	CSA24. 00MXZ040	24.00	5	5	Not required
	CST24. 00MXW0H1		Built-in	Built-in	Not required
	CSA32. 00MXZ040	32.00	5	5	Not required
	CST32. 00MXW040		Built-in	Built-in	Not required
TDK Corporation	FCR4.0 MC5	4.00	Built-in	Built-in	Not required

- **One-time Product**

Resonator manufacturer *	Resonator	Frequency (MHz)	C1 (pF)	C2 (pF)	R
Murata Mfg, Co., Ltd.	CSTCS4. 00MG0C5	4.00	Built-in	Built-in	Not required
	CST8. 00MTW	8.00	Built-in	Built-in	Not required
	CSACS8. 00MT		30	30	Not required
	CST10. 00MTZ	10.00	30	30	Not required
	CSA10. 00MTW		Built-in	Built-in	Not required
TDK Corporation	CCR4. 00MC5	4.00	Built-in	Built-in	Not required

Inquiry: Kyocera Corporation

- AVX Corporation
  North American Sales Headquarters: TEL 1-803-448-9411
- AVX LIMITED
  European Sales Headquarters: TEL 44-1252-770000
- AVX/Kyocera H.K. Ltd.
  Asian Sales Headquarters: TEL 852-363-3303

Murata Mfg. Co., Ltd.

- Murata Electronics North America, Inc.: TEL 1-404-436-1300
- Murata Europe Management GmbH: TEL 49-911-66870
- Murata Electronics Singapore (Pte.): TEL 65-758-4233

TDK Corporation

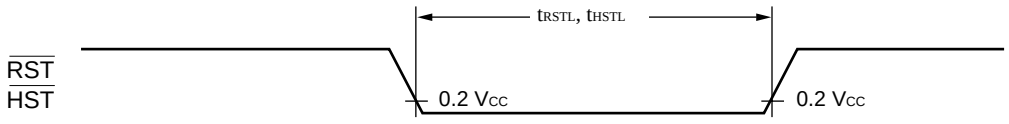
- TDK Corporation of America
  Chicago Regional Office: TEL 1-708-803-6100
- TDK Electronics Europe GmbH
  Components Division: TEL 49-2102-9450
- TDK Singapore (PTE) Ltd.: TEL 65-273-5022
- TDK Hongkong Co., Ltd.: TEL 852-736-2238
- Korea Branch, TDK Corporation: TEL 82-2-554-6636

(4) Reset and Hardware Standby Input

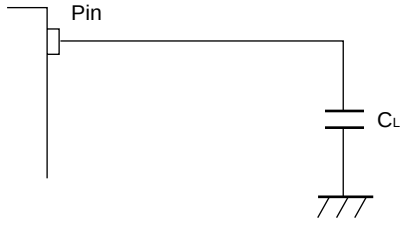
(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	$\overline{RST}$	—	16 t_{CP}	—	ns	
Hardware standby input time	t_{HSTL}	$\overline{HST}$	—	16 t_{CP}	—	ns	

Note: t_{CP} is the internal operating clock cycle time (unit: ns).



- **AC Characteristics Measurement Conditions**



C_L : Load capacitance at testing

For CLK and ALE, C_L = 30 pF
For the address/data bus, (AD15 to AD00), $\overline{RD}$, and $\overline{WR}$, C_L = 80 pF

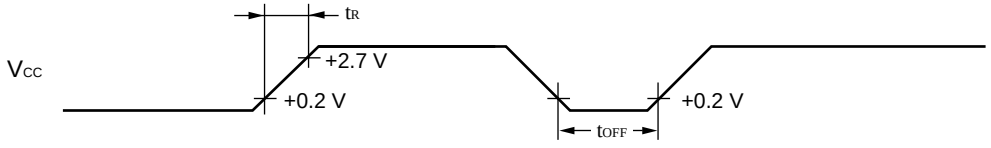
(5) Power-on Reset

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

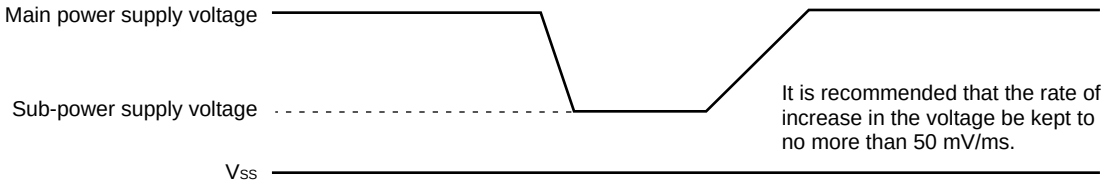
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Power supply rising time	t_R	V_{CC}	—	—	30	ms	*
Power supply cut-off time	t_{OFF}	V_{CC}	—	1	—	ms	Due to repeat operation

* : Before the power rising, V_{CC} must be less than +0.2 V.

Notes:
- The above standards are the values needed in order to activate a power-on reset.
- When $\overline{HST}$ = "L", be sure to turn on the power in accordance with these standards and apply a power-on reset, regardless of whether a power-on reset is needed or not.
- Some of the on-chip registers in a device are initialized only by a power-on reset. In order to initialize these registers, it is necessary to apply power in accordance with these standards.



If power supply voltage needs to be changed in the course of operation, a smooth voltage rise is recommended by suppressing the voltage variation as shown below.

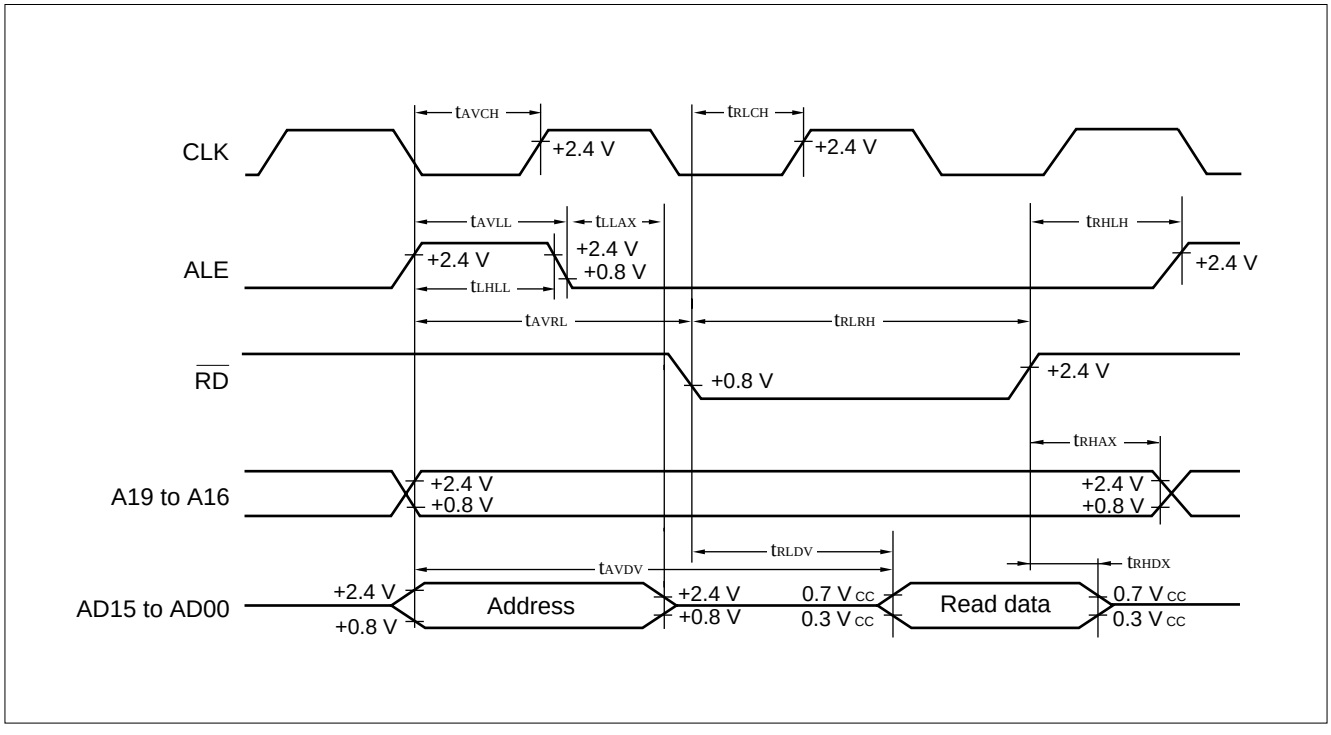


(6) Bus Read Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
ALE pulse width	t_{LHLL}	ALE	V_{CC} = +5.0 V ±10%	$t_{CP}/2$ – 20	—	ns	
			V_{CC} = +3.0 V ±10%	$t_{CP}/2$ – 35	—	ns	
Valid address → ALE ↓ time	t_{AVLL}	AD15 to AD00	V_{CC} = +5.0 V ±10%	$t_{CP}/2$ – 25	—	ns	
			V_{CC} = +3.0 V ±10%	$t_{CP}/2$ – 40	—	ns	
ALE ↓ → address valid time	t_{LLAX}	AD15 to AD00	—	$t_{CP}/2$ – 15	—	ns	
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	AD15 to AD00	—	t_{CP} – 15	—	ns	
Valid address → data read time	t_{AVDV}	AD15 to AD00	V_{CC} = +5.0 V ±10%	—	5 $t_{CP}/2$ – 60	ns	
			V_{CC} = +3.0 V ±10%	—	5 $t_{CP}/2$ – 80	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	—	3 $t_{CP}/2$ – 20	—	ns	
$\overline{RD}$ ↓ → data read time	t_{RLDV}	AD15 to AD00	V_{CC} = +5.0 V ±10%	—	3 $t_{CP}/2$ – 60	ns	
			V_{CC} = +3.0 V ±10%	—	3 $t_{CP}/2$ – 80	ns	
$\overline{RD}$ ↑ → data hold time	t_{RHDX}	AD15 to AD00	—	0	—	ns	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE	—	$t_{CP}/2$ – 15	—	ns	
$\overline{RD}$ ↑ → address invalid time	t_{RHAX}	$\overline{RD}$, A19 to A16	—	$t_{CP}/2$ – 10	—	ns	
Valid address → CLK ↑ time	t_{AVCH}	CLK, A19 to A16	—	$t_{CP}/2$ – 20	—	ns	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK	—	$t_{CP}/2$ – 20	—	ns	

Note: t_{CP} is the internal operating clock cycle time (unit: ns).

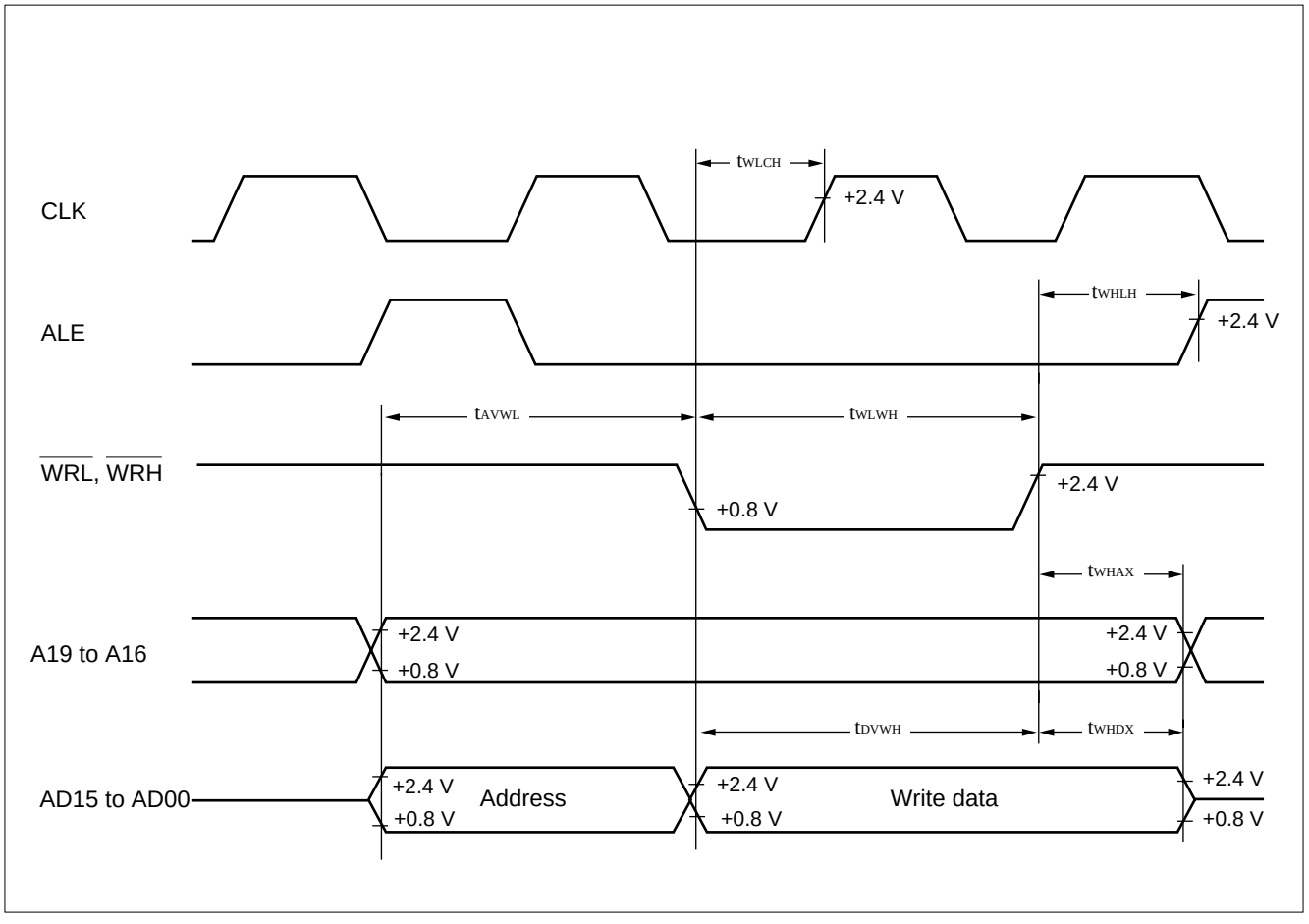


(7) Bus Write Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	A19 to A00	—	t_{CP} – 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$	—	3 t_{CP}/2 – 20	—	ns	
Write data → $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00	—	3 t_{CP}/2 – 20	—	ns	
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	AD15 to AD00	V_{CC} = +5.0 V ±10%	20	—	ns	
			V_{CC} = +3.0 V ±10%	30	—	ns	
$\overline{WR}$ ↑ → Address invalid time	t_{WHAX}	A19 to A00	—	t_{CP}/2 – 10	—	ns	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WRL}$, $\overline{WRH}$, ALE	—	t_{CP}/2 – 15	—	ns	
$\overline{WR}$ ↑ → CLK ↑ time	t_{WLCH}	$\overline{WRL}$, $\overline{WRH}$, CLK	—	t_{CP}/2 – 20	—	ns	

Note: t_{CP} is the internal operating clock cycle time (unit: ns).

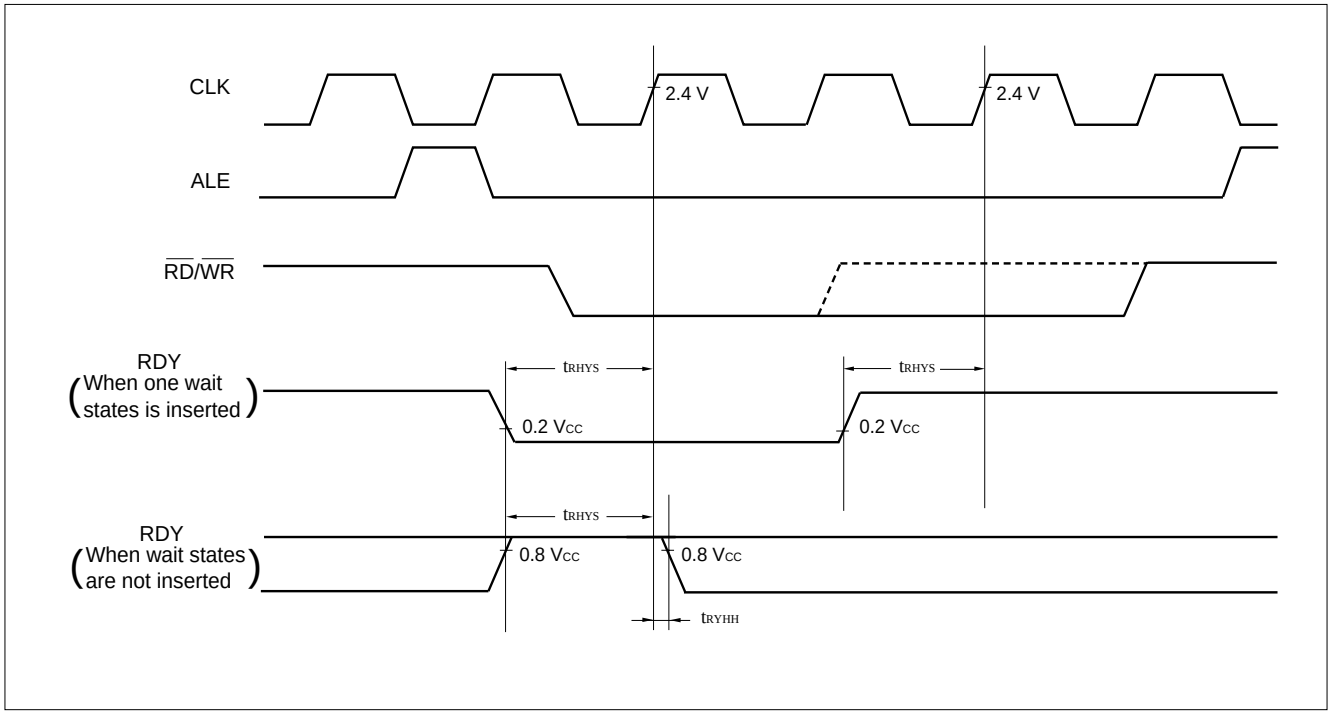


(8) Ready Input Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY setup time	t_{RYHS}	RDY	V_{CC} = +5.0 V ±10%	45	—	ns	
			V_{CC} = +3.0 V ±10%	70	—	ns	
RDY hold time	t_{RYHH}	RDY	—	0	—	ns	

Note: If the setup time during the fall of RDY is insufficient, use sthe auto ready function.

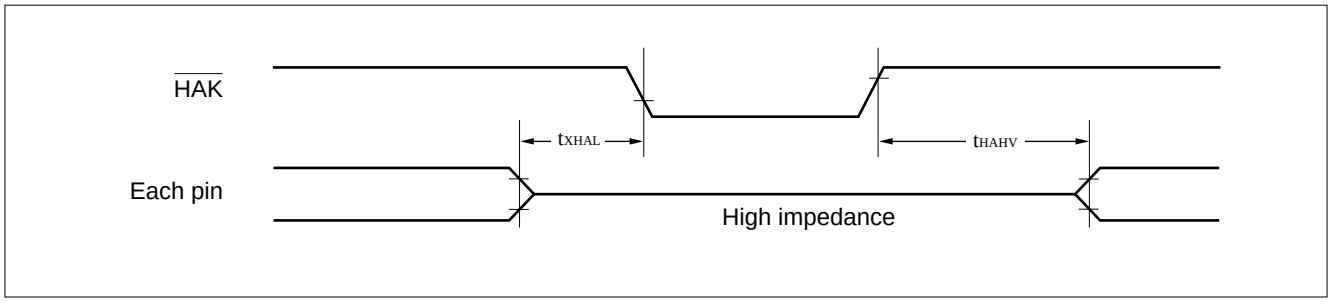


(9) Hold Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Pin floating → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns	
$\overline{HAK}$ ↑ → Pin valid time	t_{HAHV}	$\overline{HAK}$	—	t_{CP}	2 t_{CP}	ns	

Note: At least one cycle is required from the time when HRQ is fetched until $\overline{HAK}$ changes.



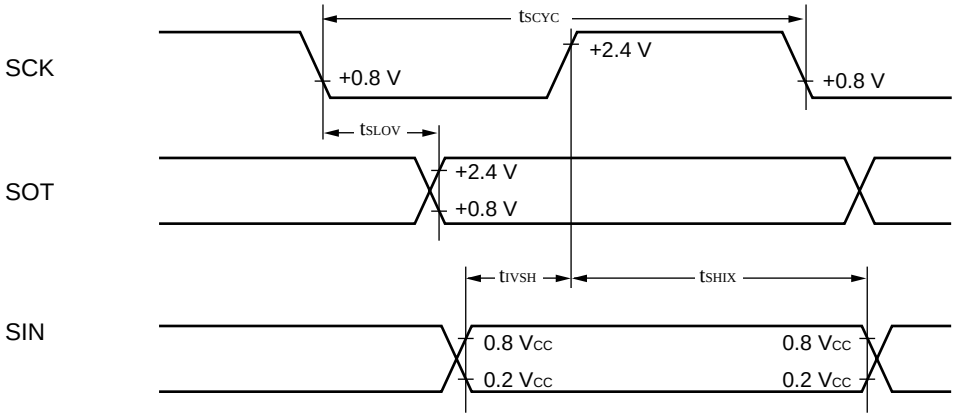
(10) UART0 Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

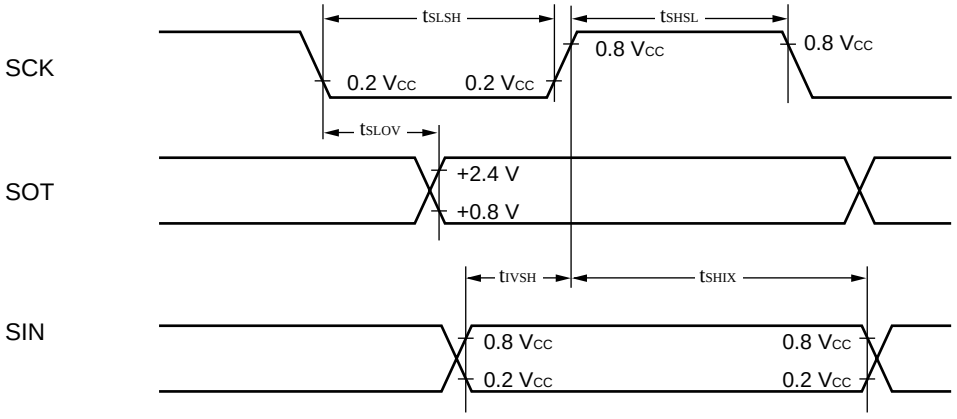
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	—	—	8 t_{CP}	—	ns	For internal shift clock mode, output pin, C_L = 80 pF + 1 TTL
SCK ↓ → SOT delay time	t_{SLOV}	—	V_{CC} = +5.0 V ±10%	–80	80	ns	
			V_{CC} = +3.0 V ±10%	–120	120	ns	
Valid SIN → SCK ↑	t_{IVSH}	—	V_{CC} = +5.0 V ±10%	100	—	ns	
			V_{CC} = +3.0 V ±10%	200	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}	—	—	t_{CP}	—	ns	
Serial clock “H” pulse width	t_{SHSL}	—	—	4 t_{CP}	—	ns	For external shift clock mode, output pin, C_L = 80 pF + 1 TTL
Serial clock “L” pulse width	t_{SLSH}	—	—	4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	—	V_{CC} = +5.0 V ±10%	—	150	ns	
			V_{CC} = +3.0 V ±10%	—	200	ns	
Valid SIN → SCK ↑	t_{IVSH}	—	V_{CC} = +5.0 V ±10%	60	—	ns	
			V_{CC} = +3.0 V ±10%	120	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}	—	V_{CC} = +5.0 V ±10%	60	—	ns	
			V_{CC} = +3.0 V ±10%	120	—	ns	

Notes: • These are the AC characteristics for CLK synchronous mode.
• C_L is the load capacitance added to pins during testing.
• t_{CP} is the internal operating clock cycle time (unit: ns).

- **Internal Shift Clock Mode**



- **External Shift Clock Mode**



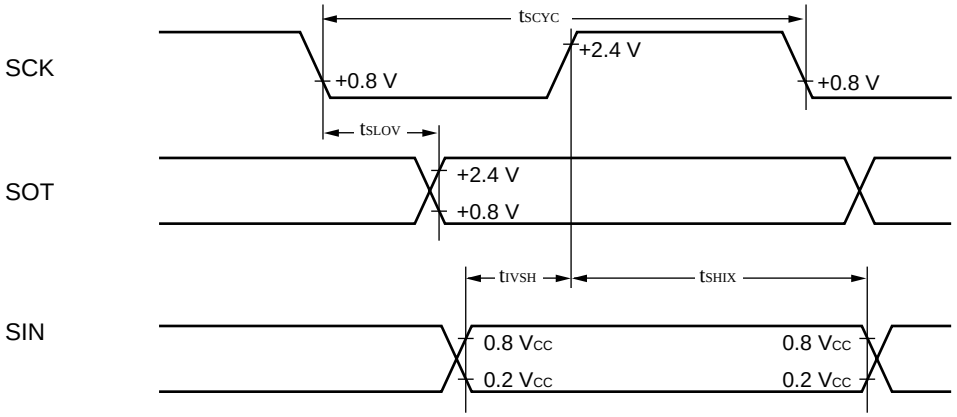
(11) UART1 Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

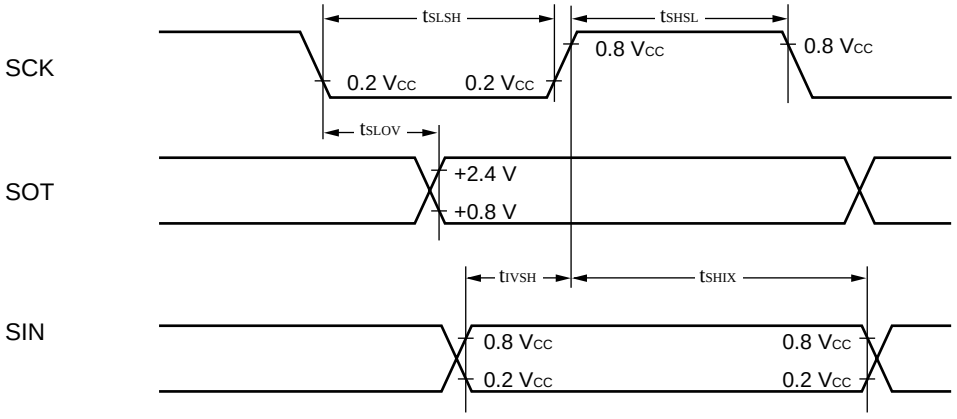
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	—	—	8 t_{CP}	—	ns	For internal shift clock mode, output pin, C_L = 80 pF + 1 TTL
SCK ↓ → SOT delay time	t_{SLOV}	—	V_{CC} = +5.0 V ±10%	–80	80	ns	
			V_{CC} = +3.0 V ±10%	–120	120	ns	
Valid SIN → SCK ↑	t_{IVSH}	—	V_{CC} = +5.0 V ±10%	100	—	ns	
			V_{CC} = +3.0 V ±10%	200	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}	—	—	t_{CP}	—	ns	
Serial clock “H” pulse width	t_{SHSL}	—	—	4 t_{CP}	—	ns	For external shift clock mode, output pin, C_L = 80 pF + 1 TTL
Serial clock “L” pulse width	t_{SLSH}	—	—	4 t_{CP}	—	ns	
SCK ↓ → SOT delay time delay time	t_{SLOV}	—	V_{CC} = +5.0 V ±10%	—	150	ns	
			V_{CC} = +3.0 V ±10%	—	200	ns	
Valid SIN → SCK ↑	t_{IVSH}	—	V_{CC} = +5.0 V ±10%	60	—	ns	
			V_{CC} = +3.0 V ±10%	120	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}	—	V_{CC} = +5.0 V ±10%	60	—	ns	
			V_{CC} = +3.0 V ±10%	120	—	ns	

Notes: • These are the AC characteristics for CLK synchronous mode.
• C_L is the load capacitance added to pins during testing.
• t_{CP} is the internal operating clock cycle time (unit: ns).

- **Internal Shift Clock Mode**



- **External Shift Clock Mode**

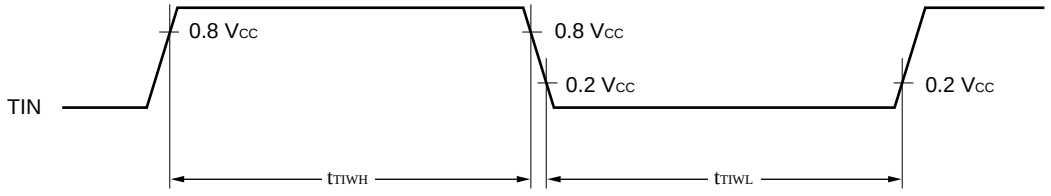


(12) Timer Input Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN1	—	4 t_{CP}	—	ns	

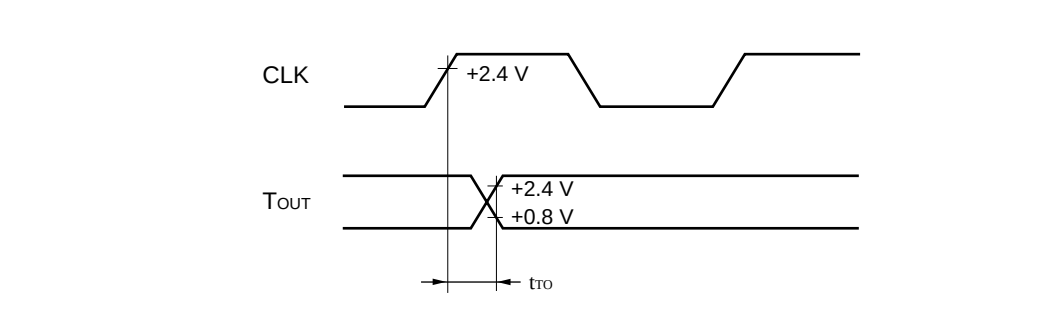
Note: t_{CP} is the internal operating clock cycle time (unit: ns).



(13) Timer Output Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
CLK ↑ → T_{OUT} change time	t_{TO}	TOT0 to TOT1	V_{CC} = +5.0 V ±10%	30	—	ns	
			V_{CC} = +3.0 V ±10%	80	—	ns	

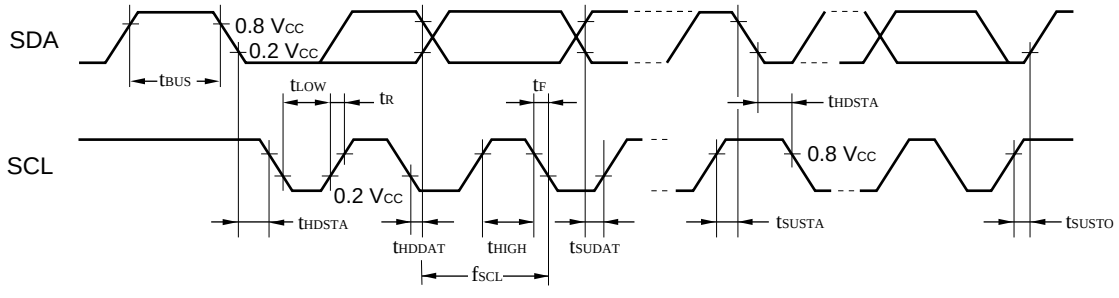


(14) I²C Timing

(V_{CC} = +2.7 V to +5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
SCL clock frequency	f_{SCL}	—	—	0	100	kHz	
Bus free time between stop and start conditions	t_{BUS}	—	—	4.7	—	µs	
Hold time (re-send) start	t_{HDSTA}	—	—	4.0	—	µs	The first clock pulse is generated after this period.
SCL clock L state hold time	t_{LOW}	—	—	4.7	—	µs	
SCL clock H state hold time	t_{HIGH}	—	—	4.0	—	µs	
Re-send start condition setup time	t_{SUSTA}	—	—	4.7	—	µs	
Data hold time	t_{HDDAT}	—	—	0	—	µs	
Data setup time	t_{SUDAT}	—	—	250	—	ns	
SDA and SCL signal rising time	t_R	—	—	—	1000	ns	
SDA and SCL signal falling time	t_F	—	—	—	300	ns	
Stop condition setup time	t_{SUSTO}	—	—	4.0	—	µs	

Note: The I²C is provided only in the MB90675 series.



5. A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC}$ = +2.7 V to +5.5 V, $AV_{SS} = V_{SS}$ = 0.0 V, +2.7 V ≦ AVRH – AVRL, T_A = –40°C to +85°C)

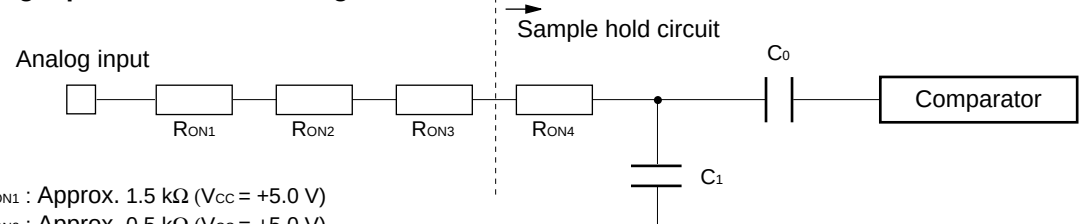
Parameter	Symbol	Pin name	Value			Unit
			Min.	Typ.	Max.	
Resolution	—	—	—	10	10	bit
Total error	—	—	—	—	±3.0	LSB
Linearity error	—	—	—	—	±2.0	LSB
Differential linearity error	—	—	—	—	±1.5	LSB
Zero transition voltage	V_{OT}	AN0 to AN7	AVRL – 1.5	AVRL + 0.5	AVRL + 2.5	LSB
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVRH – 4.5	AVRH – 1.5	AVRH + 0.5	LSB
Conversion time	—	—	6.125*1	—	—	µs
			12.25*2	—	—	µs
Analog port input current	I_{AIN}	AN0 to AN7	—	0.1	10	µA
Analog input voltage	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V
Reference voltage	—	AVRH	AVRL + 2.7	—	AV_{CC}	V
	—	AVRL	0	—	AVRH – 2.7	V
Power supply current	I_A	AV_{CC}	—	3	—	mA
	I_{AH}	AV_{CC}	—	—	5*3	µA
Reference voltage supply current	I_R	AVRH	—	200	—	µA
	I_{RH}	AVRH	—	—	5*3	µA
Interchannel disparity	—	AN0 to AN7	—	—	4	LSB

*1: When V_{CC} = +5.0 V ± 10%, and the machine clock is 16 MHz
*2: When V_{CC} = +3.0 V ± 10%, and the machine clock is 8 MHz
*3: Current when the A/D converter is not operating and the CPU is stopped (when $V_{CC} = AV_{CC}$ = AVRH = +5.0 V)

Notes: • The smaller | AVRH – AVRL |, the greater the error would become relatively.
• The output impedance of the external circuit for the analog input must satisfy the following conditions:
The output impedance of the external circuit should be less than approximately 7 kΩ.
When using an external capacitor, it is recommended to have several thousand times the capacitance of the internal capacitor as a guid, if one takes into consideration the effect of the divided capacitance between the external capacitor and the internal capacitor.

If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 3.75 µs @ at a machine clock of 16 MHz).

• **Analog Input Circuit Model Diagram**



R_{ON1} : Approx. 1.5 kΩ (V_{CC} = +5.0 V)
R_{ON2} : Approx. 0.5 kΩ (V_{CC} = +5.0 V)
R_{ON3} : Approx. 0.5 kΩ (V_{CC} = +5.0 V) C_0 : Approx. 60 pF
R_{ON4} : Approx. 0.5 kΩ (V_{CC} = +5.0 V) C_1 : Approx. 4 pF

Note: Use the values shown as guids only.

6. A/D Converter Glossary

Resolution

Analog changes that are identifiable with the A/D converter.

Linearity error

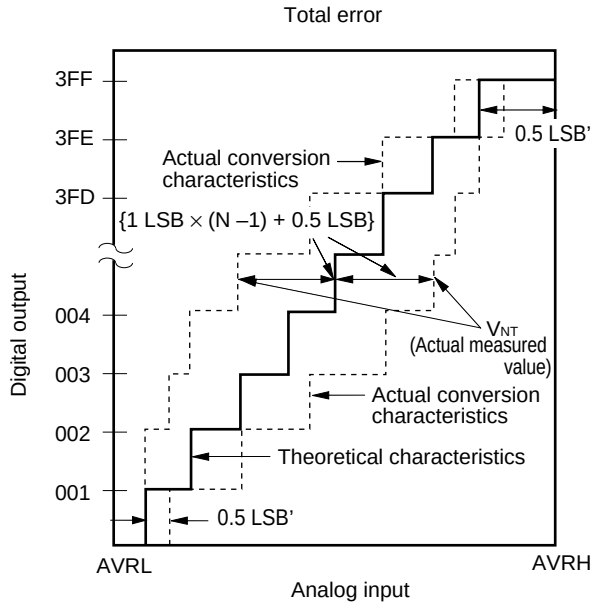
The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error

The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error

The difference between theoretical and actual conversion values caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise



$$1LSB' = (\text{Theoretical value})\ \frac{AVRH - AVRL}{1024}\ [V]$$

$$\text{Digital output N total error} = \frac{V_{NT} - \{1\ LSB' \times (N-1) + 0.5\ LSB'\}}{1\ LSB'}$$

$$V_{OT}' = (\text{Theoretical value}) = AVRL + 0.5\ LSB'\ [V]$$

$$V_{FST}' = (\text{Theoretical value}) = AVRH - 1.5\ LSB'\ [V]$$

V_{NT}: Voltage for digital output to transit from (N –1) to N

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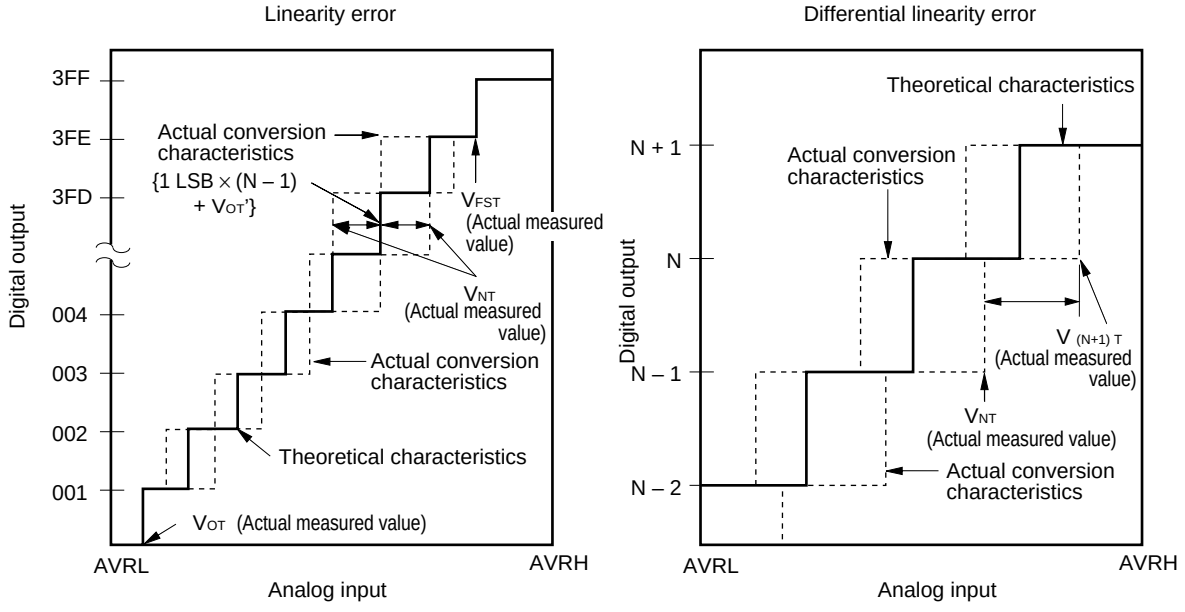
(Continued)



$$\text{Digital output N linearity error} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{OT}\}}{1\ \text{LSB'}}\ [\text{LSB}]$$

$$\text{Digital output N differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

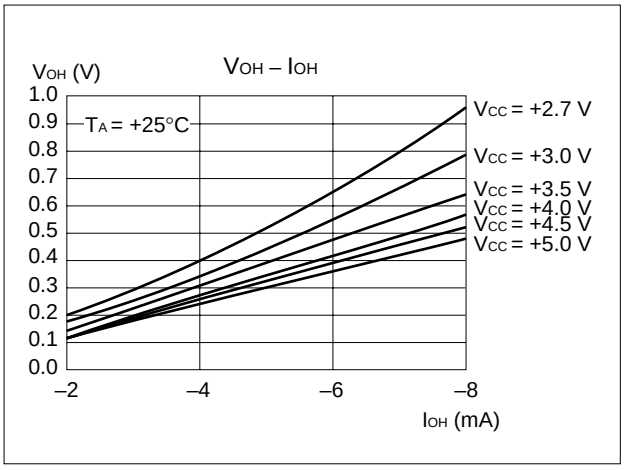
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage for digital output transit from $(000)_h$ to $(001)_h$

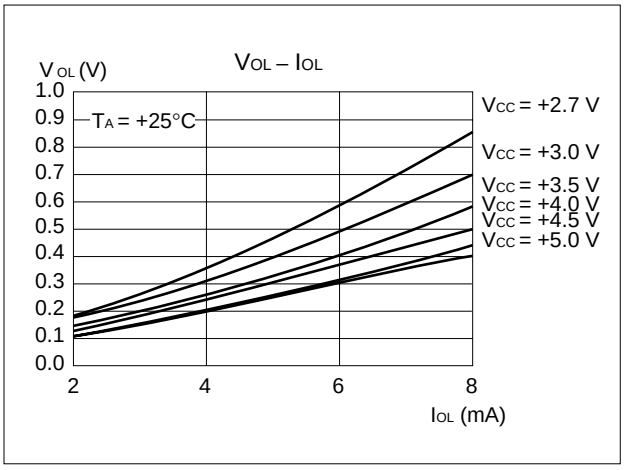
V_{FST} : Voltage for digital output transit from $(3FE)_h$ to $(3FF)_h$

■ EXAMPLE CHARACTERISTICS

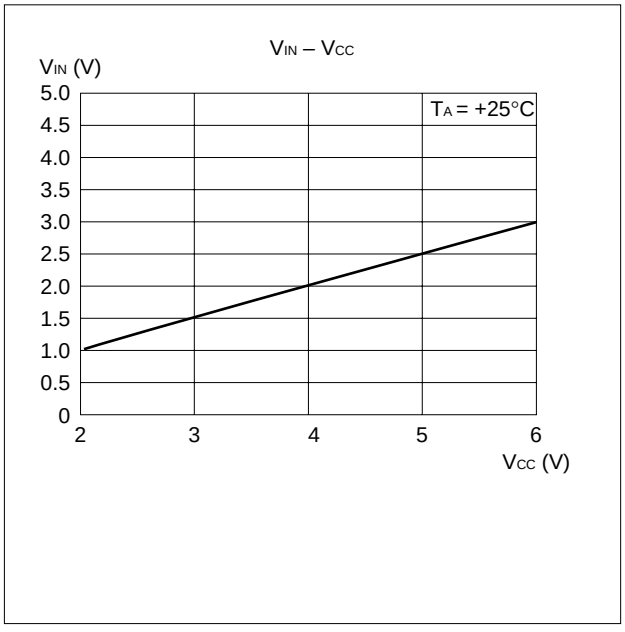
(1) “H” Level Output Voltage



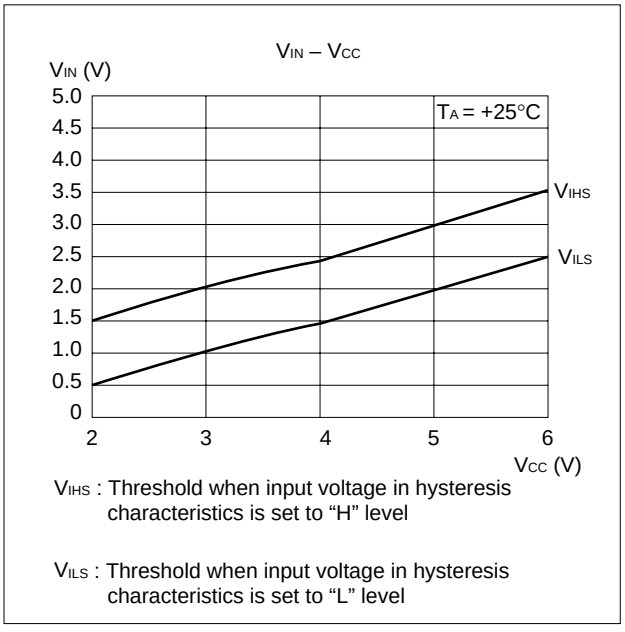
(2) “L” Level Output Voltage



(3) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)



(4) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)



VIHS : Threshold when input voltage in hysteresis characteristics is set to “H” level

VILS : Threshold when input voltage in hysteresis characteristics is set to “L” level

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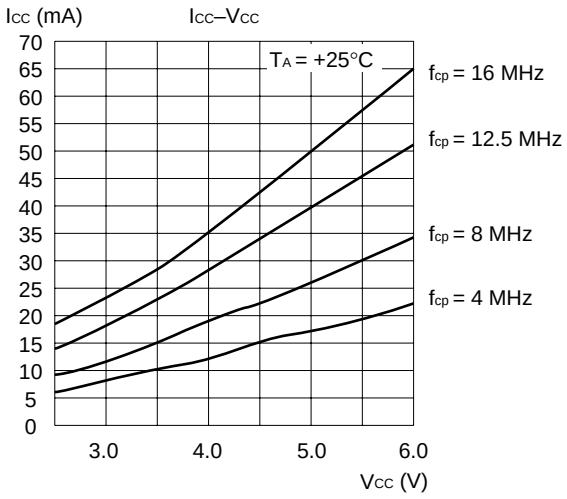
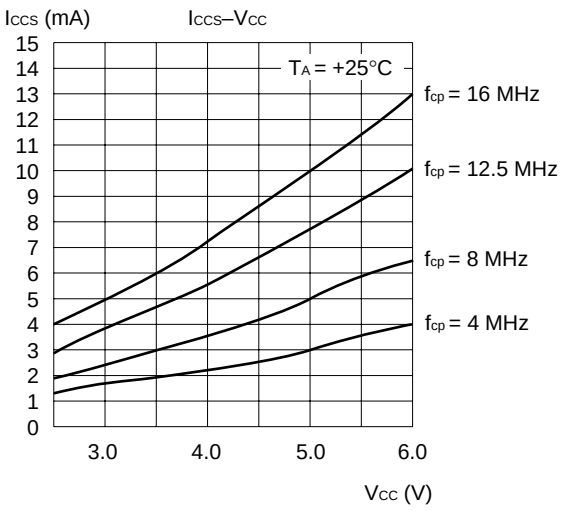
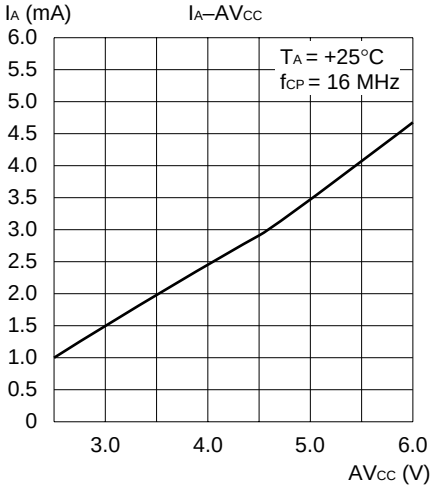
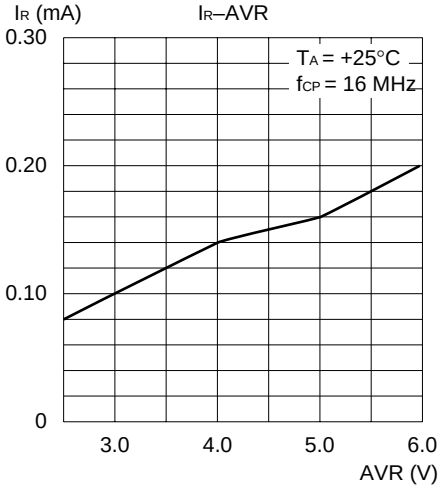
(5) Power Supply Current (f_{CP} = Internal Operating Clock Frequency)

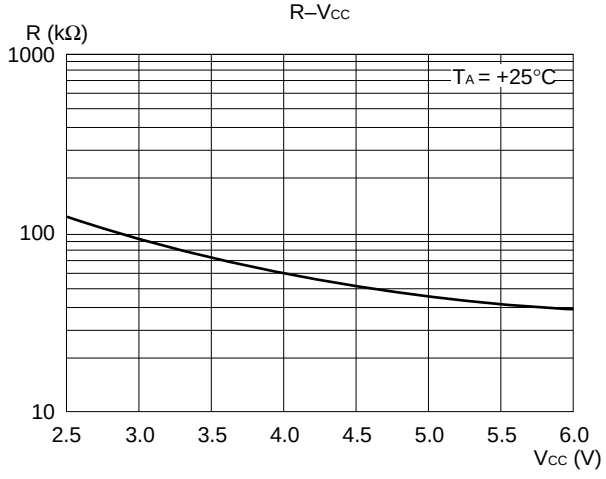








(6) Pull-up Resistance



■ INSTRUCTIONS (340 INSTRUCTIONS)

Table 1 Explanation of Items in Tables of Instructions

Item	Meaning
Mnemonic	Upper-case letters and symbols: Represented as they appear in assembler. Lower-case letters: Replaced when described in assembler. Numbers after lower-case letters: Indicate the bit width within the instruction.
#	Indicates the number of bytes.
~	Indicates the number of cycles. m : When branching n : When not branching See Table 4 for details about meanings of other letters in items.
RG	Indicates the number of accesses to the register during execution of the instruction. It is used calculate a correction value for intermittent operation of CPU.
B	Indicates the correction value for calculating the number of actual cycles during execution of the instruction. (Table 5) The number of actual cycles during execution of the instruction is the correction value summed with the value in the “~” column.
Operation	Indicates the operation of instruction.
LH	Indicates special operations involving the upper 8 bits of the lower 16 bits of the accumulator. Z : Transfers “0”. X : Extends with a sign before transferring. – : Transfers nothing.
AH	Indicates special operations involving the upper 16 bits in the accumulator. * : Transfers from AL to AH. – : No transfer. Z : Transfers 00_H to AH. X : Transfers 00_H or FF_H to AH by signing and extending AL.
I S T N Z V C	Indicates the status of each of the following flags: I (interrupt enable), S (stack), T (sticky bit), N (negative), Z (zero), V (overflow), and C (carry). * : Changes due to execution of instruction. – : No change. S : Set by execution of instruction. R : Reset by execution of instruction.
RMW	Indicates whether the instruction is a read-modify-write instruction. (a single instruction that reads data from memory, etc., processes the data, and then writes the result to memory.) * : Instruction is a read-modify-write instruction. – : Instruction is not a read-modify-write instruction. Note: A read-modify-write instruction cannot be used on addresses that have different meanings depending on whether they are read or written.

Table 2 Explanation of Symbols in Tables of Instructions

Symbol	Meaning
A	32-bit accumulator The bit length varies according to the instruction. Byte : Lower 8 bits of AL Word : 16 bits of AL Long : 32 bits of AL:AH
AH AL	Upper 16 bits of A Lower 16 bits of A
SP	Stack pointer (USP or SSP)
PC	Program counter
PCB	Program bank register
DTB	Data bank register
ADB	Additional data bank register
SSB	System stack bank register
USB	User stack bank register
SPB	Current stack bank register (SSB or USB)
DPR	Direct page register
brg1	DTB, ADB, SSB, USB, DPR, PCB, SPB
brg2	DTB, ADB, SSB, USB, DPR, SPB
Ri	R0, R1, R2, R3, R4, R5, R6, R7
RWi	RW0, RW1, RW2, RW3, RW4, RW5, RW6, RW7
RWj	RW0, RW1, RW2, RW3
RLi	RL0, RL1, RL2, RL3
dir	Compact direct addressing
addr16 addr24 ad24 0 to 15 ad24 16 to 23	Direct addressing Physical direct addressing Bit 0 to bit 15 of addr24 Bit 16 to bit 23 of addr24
io	I/O area (000000_H to $0000FF_H$)
imm4 imm8 imm16 imm32 ext (imm8)	4-bit immediate data 8-bit immediate data 16-bit immediate data 32-bit immediate data 16-bit data signed and extended from 8-bit immediate data
disp8 disp16	8-bit displacement 16-bit displacement
bp	Bit offset
vct4 vct8	Vector number (0 to 15) Vector number (0 to 255)
( )b	Bit address

(Continued)

(Continued)

Symbol	Meaning
rel	Branch specification relative to PC
ear eam	Effective addressing (codes 00 to 07) Effective addressing (codes 08 to 1F)
rlst	Register list

Table 3 Effective Address Fields

Code	Notation	Address format	Number of bytes in address extension *
00 01 02 03 04 05 06 07	R0 RW0 RL0 R1 RW1 (RL0) R2 RW2 RL1 R3 RW3 (RL1) R4 RW4 RL2 R5 RW5 (RL2) R6 RW6 RL3 R7 RW7 (RL3)	Register direct “ea” corresponds to byte, word, and long-word types, starting from the left	—
08 09 0A 0B	@RW0 @RW1 @RW2 @RW3	Register indirect	0
0C 0D 0E 0F	@RW0 + @RW1 + @RW2 + @RW3 +	Register indirect with post-increment	0
10 11 12 13 14 15 16 17	@RW0 + disp8 @RW1 + disp8 @RW2 + disp8 @RW3 + disp8 @RW4 + disp8 @RW5 + disp8 @RW6 + disp8 @RW7 + disp8	Register indirect with 8-bit displacement	1
18 19 1A 1B	@RW0 + disp16 @RW1 + disp16 @RW2 + disp16 @RW3 + disp16	Register indirect with 16-bit displacement	2
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + disp16 addr16	Register indirect with index Register indirect with index PC indirect with 16-bit displacement Direct address	0 0 2 2

Note: The number of bytes in the address extension is indicated by the “+” symbol in the “#” (number of bytes) column in the tables of instructions.

Table 4 Number of Execution Cycles for Each Type of Addressing

Code	Operand	(a) Number of execution cycles for each type of addressing	Number of register accesses for each type of addressing
00 to 07	Ri RWi RLi	Listed in tables of instructions	Listed in tables of instructions
08 to 0B	@RWj	2	1
0C to 0F	@RWj +	4	2
10 to 17	@RWi + disp8	2	1
18 to 1B	@RWj + disp16	2	1
1C 1D 1E 1F	@RW0 + RW7 @RW1 + RW7 @PC + disp16 addr16	4 4 2 1	2 2 0 0

Note: "(a)" is used in the "~" (number of states) column and column B (correction value) in the tables of instructions.

Table 5 Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles

Operand	(b) byte		(c) word		(d) long	
	Number of cycles	Number of access	Number of cycles	Number of access	Number of cycles	Number of access
Internal register	+0	1	+0	1	+0	2
Internal memory even address Internal memory odd address	+0 +0	1 1	+0 +2	1 2	+0 +4	2 4
Even address on external data bus (16 bits) Odd address on external data bus (16 bits)	+1 +1	1 1	+1 +4	1 2	+2 +8	2 4
External data bus (8 bits)	+1	1	+4	2	+8	4

Notes:
- "(b)", "(c)", and "(d)" are used in the "~" (number of states) column and column B (correction value) in the tables of instructions.
- When the external data bus is used, it is necessary to add in the number of wait cycles used for ready input and automatic ready.

Table 6 Correction Values for Number of Cycles Used to Calculate Number of Program Fetch Cycles

Instruction	Byte boundary	Word boundary
Internal memory	—	+2
External data bus (16 bits)	—	+3
External data bus (8 bits)	+3	—

Notes:
- When the external data bus is used, it is necessary to add in the number of wait cycles used for ready input and automatic ready.
- Because instruction execution is not slowed down by all program fetches in actuality, these correction values should be used for "worst case" calculations.

Table 7 Transfer Instructions (Byte) [41 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOV	A, dir	2	3	0	(b)	byte (A) ← (dir)	Z	*	–	–	–	*	*	–	–	–
MOV	A, addr16	3	4	0	(b)	byte (A) ← (addr16)	Z	*	–	–	–	*	*	–	–	–
MOV	A, Ri	1	2	1	0	byte (A) ← (Ri)	Z	*	–	–	–	*	*	–	–	–
MOV	A, ear	2	2	1	0	byte (A) ← (ear)	Z	*	–	–	–	*	*	–	–	–
MOV	A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	Z	*	–	–	–	*	*	–	–	–
MOV	A, io	2	3	0	(b)	byte (A) ← (io)	Z	*	–	–	–	*	*	–	–	–
MOV	A, #imm8	2	2	0	0	byte (A) ← imm8	Z	*	–	–	–	*	*	–	–	–
MOV	A, @A	2	3	0	(b)	byte (A) ← ((A))	Z	–	–	–	–	*	*	–	–	–
MOV	A, @RLi+disp8	3	10	2	(b)	byte (A) ← ((RLi)+disp8)	Z	*	–	–	–	*	*	–	–	–
MOVN	A, #imm4	1	1	0	0	byte (A) ← imm4	Z	*	–	–	–	R	*	–	–	–
MOVX	A, dir	2	3	0	(b)	byte (A) ← (dir)	X	*	–	–	–	*	*	–	–	–
MOVX	A, addr16	3	4	0	(b)	byte (A) ← (addr16)	X	*	–	–	–	*	*	–	–	–
MOVX	A, Ri	2	2	1	0	byte (A) ← (Ri)	X	*	–	–	–	*	*	–	–	–
MOVX	A, ear	2	2	1	0	byte (A) ← (ear)	X	*	–	–	–	*	*	–	–	–
MOVX	A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	X	*	–	–	–	*	*	–	–	–
MOVX	A, io	2	3	0	(b)	byte (A) ← (io)	X	*	–	–	–	*	*	–	–	–
MOVX	A, #imm8	2	2	0	0	byte (A) ← imm8	X	*	–	–	–	*	*	–	–	–
MOVX	A, @A	2	3	0	(b)	byte (A) ← ((A))	X	–	–	–	–	*	*	–	–	–
MOVX	A,@RWi+disp8	2	5	1	(b)	byte (A) ← ((RWi)+disp8)	X	*	–	–	–	*	*	–	–	–
MOVX	A, @RLi+disp8	3	10	2	(b)	byte (A) ← ((RLi)+disp8)	X	*	–	–	–	*	*	–	–	–
MOV	dir, A	2	3	0	(b)	byte (dir) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	addr16, A	3	4	0	(b)	byte (addr16) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	Ri, A	1	2	1	0	byte (Ri) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	ear, A	2	2	1	0	byte (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	eam, A	2+	3+ (a)	0	(b)	byte (eam) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	io, A	2	3	0	(b)	byte (io) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	@RLi+disp8, A	3	10	2	(b)	byte ((RLi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOV	Ri, ear	2	3	2	0	byte (Ri) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOV	Ri, eam	2+	4+ (a)	1	(b)	byte (Ri) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOV	ear, Ri	2	4	2	0	byte (ear) ← (Ri)	–	–	–	–	–	*	*	–	–	–
MOV	eam, Ri	2+	5+ (a)	1	(b)	byte (eam) ← (Ri)	–	–	–	–	–	*	*	–	–	–
MOV	Ri, #imm8	2	2	1	0	byte (Ri) ← imm8	–	–	–	–	–	*	*	–	–	–
MOV	io, #imm8	3	5	0	(b)	byte (io) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV	dir, #imm8	3	5	0	(b)	byte (dir) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV	ear, #imm8	3	2	1	0	byte (ear) ← imm8	–	–	–	–	–	*	*	–	–	–
MOV	eam, #imm8	3+	4+ (a)	0	(b)	byte (eam) ← imm8	–	–	–	–	–	–	–	–	–	–
MOV /MOV	@AL, AH @A, T	2	3	0	(b)	byte ((A)) ← (AH)	–	–	–	–	–	*	*	–	–	–
XCH	A, ear	2	4	2	0	byte (A) ↔ (ear)	Z	–	–	–	–	–	–	–	–	–
XCH	A, eam	2+	5+ (a)	0	2× (b)	byte (A) ↔ (eam)	Z	–	–	–	–	–	–	–	–	–
XCH	Ri, ear	2	7	4	0	byte (Ri) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCH	Ri, eam	2+	9+ (a)	2	2× (b)	byte (Ri) ↔ (eam)	–	–	–	–	–	–	–	–	–	–

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 8 Transfer Instructions (Word/Long Word) [38 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVW A, dir	2	3	0	(c)	word (A) ← (dir)	–	*	–	–	–	*	*	–	–	–
MOVW A, addr16	3	4	0	(c)	word (A) ← (addr16)	–	*	–	–	–	*	*	–	–	–
MOVW A, SP	1	1	0	0	word (A) ← (SP)	–	*	–	–	–	*	*	–	–	–
MOVW A, RWi	1	2	1	0	word (A) ← (RWi)	–	*	–	–	–	*	*	–	–	–
MOVW A, ear	2	2	1	0	word (A) ← (ear)	–	*	–	–	–	*	*	–	–	–
MOVW A, eam	2+	3+ (a)	0	(c)	word (A) ← (eam)	–	*	–	–	–	*	*	–	–	–
MOVW A, io	2	3	0	(c)	word (A) ← (io)	–	*	–	–	–	*	*	–	–	–
MOVW A, @A	2	3	0	(c)	word (A) ← ((A))	–	–	–	–	–	*	*	–	–	–
MOVW A, #imm16	3	2	0	0	word (A) ← imm16	–	*	–	–	–	*	*	–	–	–
MOVW A, @RWi+disp8	2	5	1	(c)	word (A) ← ((RWi) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVW A, @RLi+disp8	3	10	2	(c)	word (A) ← ((RLi) +disp8)	–	*	–	–	–	*	*	–	–	–
MOVW dir, A	2	3	0	(c)	word (dir) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW addr16, A	3	4	0	(c)	word (addr16) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW SP, A	1	1	0	0	word (SP) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, A	1	2	1	0	word (RWi) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW ear, A	2	2	1	0	word (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW eam, A	2+	3+ (a)	0	(c)	word (eam) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW io, A	2	3	0	(c)	word (io) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @RWi+disp8, A	2	5	1	(c)	word ((RWi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW @RLi+disp8, A	3	10	2	(c)	word ((RLi) +disp8) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, ear	2	3	2	(0)	word (RWi) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, eam	2+	4+ (a)	1	(c)	word (RWi) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVW ear, RWi	2	4	2	0	word (ear) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW eam, RWi	2+	5+ (a)	1	(c)	word (eam) ← (RWi)	–	–	–	–	–	*	*	–	–	–
MOVW RWi, #imm16	3	2	1	0	word (RWi) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW io, #imm16	4	5	0	(c)	word (io) ← imm16	–	–	–	–	–	–	–	–	–	–
MOVW ear, #imm16	4	2	1	0	word (ear) ← imm16	–	–	–	–	–	*	*	–	–	–
MOVW eam, #imm16	4+	4+ (a)	0	(c)	word (eam) ← imm16	–	–	–	–	–	–	–	–	–	–
MOVW AL, AH /MOVW @A, T	2	3	0	(c)	word ((A)) ← (AH)	–	–	–	–	–	*	*	–	–	–
XCHW A, ear	2	4	2	0	word (A) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCHW A, eam	2+	5+ (a)	0	2× (c)	word (A) ↔ (eam)	–	–	–	–	–	–	–	–	–	–
XCHW RWi, ear	2	7	4	0	word (RWi) ↔ (ear)	–	–	–	–	–	–	–	–	–	–
XCHW RWi, eam	2+	9+ (a)	2	2× (c)	word (RWi) ↔ (eam)	–	–	–	–	–	–	–	–	–	–
MOVL A, ear	2	4	2	0	long (A) ← (ear)	–	–	–	–	–	*	*	–	–	–
MOVL A, eam	2+	5+ (a)	0	(d)	long (A) ← (eam)	–	–	–	–	–	*	*	–	–	–
MOVL A, #imm32	5	3	0	0	long (A) ← imm32	–	–	–	–	–	*	*	–	–	–
MOVL ear, A	2	4	2	0	long (ear) ← (A)	–	–	–	–	–	*	*	–	–	–
MOVL eam, A	2+	5+ (a)	0	(d)	long (eam) ← (A)	–	–	–	–	–	*	*	–	–	–

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 9 Addition and Subtraction Instructions (Byte/Word/Long Word) [42 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ADD A,#imm8	2	2	0	0	byte (A) ← (A) +imm8	Z	–	–	–	–	*	*	*	*	–
ADD A, dir	2	5	0	(b)	byte (A) ← (A) +(dir)	Z	–	–	–	–	*	*	*	*	–
ADD A, ear	2	3	1	0	byte (A) ← (A) +(ear)	Z	–	–	–	–	*	*	*	*	–
ADD A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) +(eam)	Z	–	–	–	–	*	*	*	*	–
ADD ear, A	2	3	2	0	byte (ear) ← (ear) + (A)	–	–	–	–	–	*	*	*	*	–
ADD eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) + (A)	Z	–	–	–	–	*	*	*	*	*
ADDC A	1	2	0	0	byte (A) ← (AH) + (AL) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDC A, ear	2	3	1	0	byte (A) ← (A) + (ear) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDC A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) + (eam) + (C)	Z	–	–	–	–	*	*	*	*	–
ADDDC A	1	3	0	0	byte (A) ← (AH) + (AL) + (C) (decimal)	Z	–	–	–	–	*	*	*	*	–
SUB A, #imm8	2	2	0	0	byte (A) ← (A) –imm8	Z	–	–	–	–	*	*	*	*	–
SUB A, dir	2	5	0	(b)	byte (A) ← (A) – (dir)	Z	–	–	–	–	*	*	*	*	–
SUB A, ear	2	3	1	0	byte (A) ← (A) – (ear)	Z	–	–	–	–	*	*	*	*	–
SUB A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) – (eam)	Z	–	–	–	–	*	*	*	*	–
SUB ear, A	2	3	2	0	byte (ear) ← (ear) – (A)	–	–	–	–	–	*	*	*	*	–
SUB eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) – (A)	–	–	–	–	–	*	*	*	*	*
SUBC A	1	2	0	0	byte (A) ← (AH) – (AL) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBC A, ear	2	3	1	0	byte (A) ← (A) – (ear) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBC A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) – (eam) – (C)	Z	–	–	–	–	*	*	*	*	–
SUBDC A	1	3	0	0	byte (A) ← (AH) – (AL) – (C) (decimal)	Z	–	–	–	–	*	*	*	*	–
ADDW A	1	2	0	0	word (A) ← (AH) + (AL)	–	–	–	–	–	*	*	*	*	–
ADDW A, ear	2	3	1	0	word (A) ← (A) +(ear)	–	–	–	–	–	*	*	*	*	–
ADDW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) +(eam)	–	–	–	–	–	*	*	*	*	–
ADDW A, #imm16	3	2	0	0	word (A) ← (A) +imm16	–	–	–	–	–	*	*	*	*	–
ADDW ear, A	2	3	2	0	word (ear) ← (ear) + (A)	–	–	–	–	–	*	*	*	*	–
ADDW eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) + (A)	–	–	–	–	–	*	*	*	*	*
ADDCW A, ear	2	3	1	0	word (A) ← (A) + (ear) + (C)	–	–	–	–	–	*	*	*	*	–
ADDCW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) + (eam) + (C)	–	–	–	–	–	*	*	*	*	–
SUBW A	1	2	0	0	word (A) ← (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
SUBW A, ear	2	3	1	0	word (A) ← (A) – (ear)	–	–	–	–	–	*	*	*	*	–
SUBW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) – (eam)	–	–	–	–	–	*	*	*	*	–
SUBW A, #imm16	3	2	0	0	word (A) ← (A) –imm16	–	–	–	–	–	*	*	*	*	–
SUBW ear, A	2	3	2	0	word (ear) ← (ear) – (A)	–	–	–	–	–	*	*	*	*	–
SUBW eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) – (A)	–	–	–	–	–	*	*	*	*	*
SUBCW A, ear	2	3	1	0	word (A) ← (A) – (ear) – (C)	–	–	–	–	–	*	*	*	*	–
SUBCW A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) – (eam) – (C)	–	–	–	–	–	*	*	*	*	–
ADDL A, ear	2	6	2	0	long (A) ← (A) + (ear)	–	–	–	–	–	*	*	*	*	–
ADDL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) + (eam)	–	–	–	–	–	*	*	*	*	–
ADDL A, #imm32	5	4	0	0	long (A) ← (A) +imm32	–	–	–	–	–	*	*	*	*	–
SUBL A, ear	2	6	2	0	long (A) ← (A) – (ear)	–	–	–	–	–	*	*	*	*	–
SUBL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) – (eam)	–	–	–	–	–	*	*	*	*	–
SUBL A, #imm32	5	4	0	0	long (A) ← (A) –imm32	–	–	–	–	–	*	*	*	*	–

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 10 Increment and Decrement Instructions (Byte/Word/Long Word) [12 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
INC	ear	2	2	2	0	byte (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INC	eam	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DEC	ear	2	3	2	0	byte (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DEC	eam	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCW	ear	2	3	2	0	word (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INCW	eam	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECW	ear	2	3	2	0	word (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DECW	eam	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*
INCL	ear	2	7	4	0	long (ear) ← (ear) +1	–	–	–	–	–	*	*	*	–	–
INCL	eam	2+	9+ (a)	0	2× (d)	long (eam) ← (eam) +1	–	–	–	–	–	*	*	*	–	*
DECL	ear	2	7	4	0	long (ear) ← (ear) –1	–	–	–	–	–	*	*	*	–	–
DECL	eam	2+	9+ (a)	0	2× (d)	long (eam) ← (eam) –1	–	–	–	–	–	*	*	*	–	*

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 11 Compare Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CMP	A	1	1	0	0	byte (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMP	A, ear	2	2	1	0	byte (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMP	A, eam	2+	3+ (a)	0	(b)	byte (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMP	A, #imm8	2	2	0	0	byte (A) ← imm8	–	–	–	–	–	*	*	*	*	–
CMPW	A	1	1	0	0	word (AH) – (AL)	–	–	–	–	–	*	*	*	*	–
CMPW	A, ear	2	2	1	0	word (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMPW	A, eam	2+	3+ (a)	0	(c)	word (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMPW	A, #imm16	3	2	0	0	word (A) ← imm16	–	–	–	–	–	*	*	*	*	–
CMPL	A, ear	2	6	2	0	word (A) ← (ear)	–	–	–	–	–	*	*	*	*	–
CMPL	A, eam	2+	7+ (a)	0	(d)	word (A) ← (eam)	–	–	–	–	–	*	*	*	*	–
CMPL	A, #imm32	5	3	0	0	word (A) ← imm32	–	–	–	–	–	*	*	*	*	–

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 12 Multiplication and Division Instructions (Byte/Word/Long Word) [11 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
DIVU	A	1	*1	0	0	word (AH) /byte (AL) Quotient → byte (AL) Remainder → byte (AH)	–	–	–	–	–	–	–	*	*	–
DIVU	A, ear	2	*2	1	0	word (A)/byte (ear) Quotient → byte (A) Remainder → byte (ear)	–	–	–	–	–	–	–	*	*	–
DIVU	A, eam	2+	*3	0	*6	word (A)/byte (eam) Quotient → byte (A) Remainder → byte (eam)	–	–	–	–	–	–	–	*	*	–
DIVUW	A, ear	2	*4	1	0	long (A)/word (ear) Quotient → word (A) Remainder → word (ear)	–	–	–	–	–	–	–	*	*	–
DIVUW	A, eam	2+	*5	0	*7	long (A)/word (eam) Quotient → word (A) Remainder → word (eam)	–	–	–	–	–	–	–	*	*	–
MULU	A	1	*8	0	0	byte (AH) *byte (AL) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU	A, ear	2	*9	1	0	byte (A) *byte (ear) → word (A)	–	–	–	–	–	–	–	–	–	–
MULU	A, eam	2+	*10	0	(b)	byte (A) *byte (eam) → word (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A	1	*11	0	0	word (AH) *word (AL) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A, ear	2	*12	1	0	word (A) *word (ear) → long (A)	–	–	–	–	–	–	–	–	–	–
MULUW	A, eam	2+	*13	0	(c)	word (A) *word (eam) → long (A)	–	–	–	–	–	–	–	–	–	–

*1: 3 when the result is zero, 7 when an overflow occurs, and 15 normally.
*2: 4 when the result is zero, 8 when an overflow occurs, and 16 normally.
*3: 6 + (a) when the result is zero, 9 + (a) when an overflow occurs, and 19 + (a) normally.
*4: 4 when the result is zero, 7 when an overflow occurs, and 22 normally.
*5: 6 + (a) when the result is zero, 8 + (a) when an overflow occurs, and 26 + (a) normally.
*6: (b) when the result is zero or when an overflow occurs, and 2 × (b) normally.
*7: (c) when the result is zero or when an overflow occurs, and 2 × (c) normally.
*8: 3 when byte (AH) is zero, and 7 when byte (AH) is not zero.
*9: 4 when byte (ear) is zero, and 8 when byte (ear) is not zero.
*10: 5 + (a) when byte (eam) is zero, and 9 + (a) when byte (eam) is not 0.
*11: 3 when word (AH) is zero, and 11 when word (AH) is not zero.
*12: 4 when word (ear) is zero, and 12 when word (ear) is not zero.
*13: 5 + (a) when word (eam) is zero, and 13 + (a) when word (eam) is not zero.

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 13 Logical 1 Instructions (Byte/Word) [39 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
AND	A, #imm8	2	2	0	0	byte (A) ← (A) and imm8	–	–	–	–	–	*	*	R	–	–
AND	A, ear	2	3	1	0	byte (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
AND	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
AND	ear, A	2	3	2	0	byte (ear) ← (ear) and (A)	–	–	–	–	–	*	*	R	–	–
AND	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) and (A)	–	–	–	–	–	*	*	R	–	*
OR	A, #imm8	2	2	0	0	byte (A) ← (A) or imm8	–	–	–	–	–	*	*	R	–	–
OR	A, ear	2	3	1	0	byte (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
OR	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
OR	ear, A	2	3	2	0	byte (ear) ← (ear) or (A)	–	–	–	–	–	*	*	R	–	–
OR	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) or (A)	–	–	–	–	–	*	*	R	–	*
XOR	A, #imm8	2	2	0	0	byte (A) ← (A) xor imm8	–	–	–	–	–	*	*	R	–	–
XOR	A, ear	2	3	1	0	byte (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XOR	A, eam	2+	4+ (a)	0	(b)	byte (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–
XOR	ear, A	2	3	2	0	byte (ear) ← (ear) xor (A)	–	–	–	–	–	*	*	R	–	–
XOR	eam, A	2+	5+ (a)	0	2× (b)	byte (eam) ← (eam) xor (A)	–	–	–	–	–	*	*	R	–	*
NOT	A	1	2	0	0	byte (A) ← not (A)	–	–	–	–	–	*	*	R	–	–
NOT	ear	2	3	2	0	byte (ear) ← not (ear)	–	–	–	–	–	*	*	R	–	–
NOT	eam	2+	5+ (a)	0	2× (b)	byte (eam) ← not (eam)	–	–	–	–	–	*	*	R	–	*
ANDW	A	1	2	0	0	word (A) ← (AH) and (A)	–	–	–	–	–	*	*	R	–	–
ANDW	A, #imm16	3	2	0	0	word (A) ← (A) and imm16	–	–	–	–	–	*	*	R	–	–
ANDW	A, ear	2	3	1	0	word (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
ANDW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
ANDW	ear, A	2	3	2	0	word (ear) ← (ear) and (A)	–	–	–	–	–	*	*	R	–	–
ANDW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) and (A)	–	–	–	–	–	*	*	R	–	*
ORW	A	1	2	0	0	word (A) ← (AH) or (A)	–	–	–	–	–	*	*	R	–	–
ORW	A, #imm16	3	2	0	0	word (A) ← (A) or imm16	–	–	–	–	–	*	*	R	–	–
ORW	A, ear	2	3	1	0	word (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
ORW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
ORW	ear, A	2	3	2	0	word (ear) ← (ear) or (A)	–	–	–	–	–	*	*	R	–	–
ORW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) or (A)	–	–	–	–	–	*	*	R	–	*
XORW	A	1	2	0	0	word (A) ← (AH) xor (A)	–	–	–	–	–	*	*	R	–	–
XORW	A, #imm16	3	2	0	0	word (A) ← (A) xor imm16	–	–	–	–	–	*	*	R	–	–
XORW	A, ear	2	3	1	0	word (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XORW	A, eam	2+	4+ (a)	0	(c)	word (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–
XORW	ear, A	2	3	2	0	word (ear) ← (ear) xor (A)	–	–	–	–	–	*	*	R	–	–
XORW	eam, A	2+	5+ (a)	0	2× (c)	word (eam) ← (eam) xor (A)	–	–	–	–	–	*	*	R	–	*
NOTW	A	1	2	0	0	word (A) ← not (A)	–	–	–	–	–	*	*	R	–	–
NOTW	ear	2	3	2	0	word (ear) ← not (ear)	–	–	–	–	–	*	*	R	–	–
NOTW	eam	2+	5+ (a)	0	2× (c)	word (eam) ← not (eam)	–	–	–	–	–	*	*	R	–	*

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 14 Logical 2 Instructions (Long Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
ANDL A, ear	2	6	2	0	long (A) ← (A) and (ear)	–	–	–	–	–	*	*	R	–	–
ANDL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) and (eam)	–	–	–	–	–	*	*	R	–	–
ORL A, ear	2	6	2	0	long (A) ← (A) or (ear)	–	–	–	–	–	*	*	R	–	–
ORL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) or (eam)	–	–	–	–	–	*	*	R	–	–
XORL A, ea	2	6	2	0	long (A) ← (A) xor (ear)	–	–	–	–	–	*	*	R	–	–
XORL A, eam	2+	7+ (a)	0	(d)	long (A) ← (A) xor (eam)	–	–	–	–	–	*	*	R	–	–

Table 15 Sign Inversion Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NEG A	1	2	0	0	byte (A) ← 0 – (A)	X	–	–	–	–	*	*	*	*	–
NEG ear	2	3	2	0	byte (ear) ← 0 – (ear)	–	–	–	–	–	*	*	*	*	–
NEG eam	2+	5+ (a)	0	2× (b)	byte (eam) ← 0 – (eam)	–	–	–	–	–	*	*	*	*	*
NEGW A	1	2	0	0	word (A) ← 0 – (A)	–	–	–	–	–	*	*	*	*	–
NEGW ear	2	3	2	0	word (ear) ← 0 – (ear)	–	–	–	–	–	*	*	*	*	–
NEGW eam	2+	5+ (a)	0	2× (c)	word (eam) ← 0 – (eam)	–	–	–	–	–	*	*	*	*	*

Table 16 Normalize Instruction (Long Word) [1 Instruction]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
NRML A, R0	2	*1	1	0	long (A) ← Shift until first digit is "1" byte (R0) ← Current shift count	–	–	–	–	–	–	*	–	–	–

*1: 4 when the contents of the accumulator are all zeroes, 6 + (R0) in all other cases (shift count).

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 17 Shift Instructions (Byte/Word/Long Word) [18 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
RORC A	2	2	0	0	byte (A) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	–
ROLC A	2	2	0	0	byte (A) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	–
RORC ear	2	3	2	0	byte (ear) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	–
RORC eam	2+	5+ (a)	0	2× (b)	byte (eam) ← Right rotation with carry	–	–	–	–	–	*	*	–	*	*
ROLC ear	2	3	2	0	byte (ear) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	–
ROLC eam	2+	5+ (a)	0	2× (b)	byte (eam) ← Left rotation with carry	–	–	–	–	–	*	*	–	*	*
ASR A, R0	2	*1	1	0	byte (A) ← Arithmetic right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSR A, R0	2	*1	1	0	byte (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSL A, R0	2	*1	1	0	byte (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–
ASRW A	1	2	0	0	word (A) ← Arithmetic right shift (A, 1 bit)	–	–	–	–	*	*	*	–	*	–
LSRW A/SHRW A	1	2	0	0	word (A) ← Logical right shift (A, 1 bit)	–	–	–	–	*	R	*	–	*	–
LSLW A/SHLW A	1	2	0	0	word (A) ← Logical left shift (A, 1 bit)	–	–	–	–	–	*	*	–	*	–
ASRW A, R0	2	*1	1	0	word (A) ← Arithmetic right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSRW A, R0	2	*1	1	0	word (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSLW A, R0	2	*1	1	0	word (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–
ASRL A, R0	2	*2	1	0	long (A) ← Arithmetic right shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSRL A, R0	2	*2	1	0	long (A) ← Logical right barrel shift (A, R0)	–	–	–	–	*	*	*	–	*	–
LSLL A, R0	2	*2	1	0	long (A) ← Logical left barrel shift (A, R0)	–	–	–	–	–	*	*	–	*	–

*1: 6 when R0 is 0, 5 + (R0) in all other cases.
*2: 6 when R0 is 0, 6 + (R0) in all other cases.

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 18 Branch 1 Instructions [31 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
BZ/BEQ rel	2	*1	0	0	Branch when (Z) = 1	–	–	–	–	–	–	–	–	–	–
BNZ/BNE rel	2	*1	0	0	Branch when (Z) = 0	–	–	–	–	–	–	–	–	–	–
BC/BLO rel	2	*1	0	0	Branch when (C) = 1	–	–	–	–	–	–	–	–	–	–
BNC/BHS rel	2	*1	0	0	Branch when (C) = 0	–	–	–	–	–	–	–	–	–	–
BN rel	2	*1	0	0	Branch when (N) = 1	–	–	–	–	–	–	–	–	–	–
BP rel	2	*1	0	0	Branch when (N) = 0	–	–	–	–	–	–	–	–	–	–
BV rel	2	*1	0	0	Branch when (V) = 1	–	–	–	–	–	–	–	–	–	–
BNV rel	2	*1	0	0	Branch when (V) = 0	–	–	–	–	–	–	–	–	–	–
BT rel	2	*1	0	0	Branch when (T) = 1	–	–	–	–	–	–	–	–	–	–
BNT rel	2	*1	0	0	Branch when (T) = 0	–	–	–	–	–	–	–	–	–	–
BLT rel	2	*1	0	0	Branch when (V) xor (N) = 1	–	–	–	–	–	–	–	–	–	–
BGE rel	2	*1	0	0	Branch when (V) xor (N) = 0	–	–	–	–	–	–	–	–	–	–
BLE rel	2	*1	0	0	Branch when ((V) xor (N)) or (Z) = 1	–	–	–	–	–	–	–	–	–	–
BGT rel	2	*1	0	0	Branch when ((V) xor (N)) or (Z) = 0	–	–	–	–	–	–	–	–	–	–
BLS rel	2	*1	0	0	Branch when (C) or (Z) = 1	–	–	–	–	–	–	–	–	–	–
BHI rel	2	*1	0	0	Branch when (C) or (Z) = 0	–	–	–	–	–	–	–	–	–	–
BRA rel	2	*1	0	0	Branch unconditionally	–	–	–	–	–	–	–	–	–	–
JMP @A	1	2	0	0	word (PC) ← (A)	–	–	–	–	–	–	–	–	–	–
JMP addr16	3	3	0	0	word (PC) ← addr16	–	–	–	–	–	–	–	–	–	–
JMP @ear	2	3	1	0	word (PC) ← (ear)	–	–	–	–	–	–	–	–	–	–
JMP @eam	2+	4+ (a)	0	(c)	word (PC) ← (eam)	–	–	–	–	–	–	–	–	–	–
JMPP @ear *3	2	5	2	0	word (PC) ← (ear), (PCB) ← (ear +2)	–	–	–	–	–	–	–	–	–	–
JMPP @eam *3	2+	6+ (a)	0	(d)	word (PC) ← (eam), (PCB) ← (eam +2)	–	–	–	–	–	–	–	–	–	–
JMPP addr24	4	4	0	0	word (PC) ← ad24 0 to 15, (PCB) ← ad24 16 to 23	–	–	–	–	–	–	–	–	–	–
CALL @ear *4	2	6	1	(c)	word (PC) ← (ear)	–	–	–	–	–	–	–	–	–	–
CALL @eam *4	2+	7+ (a)	0	2× (c)	word (PC) ← (eam)	–	–	–	–	–	–	–	–	–	–
CALL addr16 *5	3	6	0	(c)	word (PC) ← addr16	–	–	–	–	–	–	–	–	–	–
CALLV #vct4 *5	1	7	0	2× (c)	Vector call instruction	–	–	–	–	–	–	–	–	–	–
CALLP @ear *6	2	10	2	2× (c)	word (PC) ← (ear) 0 to 15 (PCB) ← (ear) 16 to 23	–	–	–	–	–	–	–	–	–	–
CALLP @eam *6	2+	11+ (a)	0	*2	word (PC) ← (eam) 0 to 15 (PCB) ← (eam) 16 to 23	–	–	–	–	–	–	–	–	–	–
CALLP addr24 *7	4	10	0	2× (c)	word (PC) ← addr0 to 15, (PCB) ← addr16 to 23	–	–	–	–	–	–	–	–	–	–

*1: 4 when branching, 3 when not branching.
*2: (b) + 3 × (c)
*3: Read (word) branch address.
*4: W: Save (word) to stack; R: read (word) branch address.
*5: Save (word) to stack.
*6: W: Save (long word) to W stack; R: read (long word) R branch address.
*7: Save (long word) to stack.

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 19 Branch 2 Instructions [19 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
CBNE A, #imm8, rel	3	*1	0	0	Branch when byte (A) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CWBNE A, #imm16, rel	4	*1	0	0	Branch when word (A) ≠ imm16	–	–	–	–	–	*	*	*	*	–
CBNE ear, #imm8, rel	4	*2	1	0	Branch when byte (ear) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CBNE eam, #imm8, rel*9	4+	*3	0	(b)	Branch when byte (eam) ≠ imm8	–	–	–	–	–	*	*	*	*	–
CWBNE ear, #imm16, rel	5	*4	1	0	Branch when word (ear) ≠ imm16	–	–	–	–	–	*	*	*	*	–
CWBNE eam, #imm16, rel*9	5+	*3	0	(c)	Branch when word (eam) ≠ imm16	–	–	–	–	–	*	*	*	*	–
DBNZ ear, rel	3	*5	2	0	Branch when byte (ear) = (ear) – 1, and (ear) ≠ 0	–	–	–	–	–	*	*	*	–	–
DBNZ eam, rel	3+	*6	2	2× (b)	Branch when byte (eam) = (eam) – 1, and (eam) ≠ 0	–	–	–	–	–	*	*	*	–	*
DWBNZ ear, rel	3	*5	2	0	Branch when word (ear) = (ear) – 1, and (ear) ≠ 0	–	–	–	–	–	*	*	*	–	–
DWBNZ eam, rel	3+	*6	2	2× (c)	Branch when word (eam) = (eam) – 1, and (eam) ≠ 0	–	–	–	–	–	*	*	*	–	*
INT #vct8	2	20	0	8× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INT addr16	3	16	0	6× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INTP addr24	4	17	0	6× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
INT9	1	20	0	8× (c)	Software interrupt	–	–	R	S	–	–	–	–	–	–
RETI	1	15	0	6× (c)	Return from interrupt	–	–	*	*	*	*	*	*	*	–
LINK #local8	2	6	0	(c)	At constant entry, save old frame pointer to stack, set new frame pointer, and allocate local pointer area	–	–	–	–	–	–	–	–	–	–
UNLINK	1	5	0	(c)	At constant entry, retrieve old frame pointer from stack.	–	–	–	–	–	–	–	–	–	–
RET *7	1	4	0	(c)	Return from subroutine	–	–	–	–	–	–	–	–	–	–
RETP *8	1	6	0	(d)	Return from subroutine	–	–	–	–	–	–	–	–	–	–

*1: 5 when branching, 4 when not branching
*2: 13 when branching, 12 when not branching
*3: 7 + (a) when branching, 6 + (a) when not branching
*4: 8 when branching, 7 when not branching
*5: 7 when branching, 6 when not branching
*6: 8 + (a) when branching, 7 + (a) when not branching
*7: Retrieve (word) from stack
*8: Retrieve (long word) from stack
*9: In the CBNE/CWBNE instruction, do not use the RWj+ addressing mode.

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 20 Other Control Instructions (Byte/Word/Long Word) [36 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
PUSHW A	1	4	0	(c)	word (SP) ← (SP) –2, ((SP)) ← (A)	–	–	–	–	–	–	–	–	–	–
PUSHW AH	1	4	0	(c)	word (SP) ← (SP) –2, ((SP)) ← (AH)	–	–	–	–	–	–	–	–	–	–
PUSHW PS	1	4	0	(c)	word (SP) ← (SP) –2, ((SP)) ← (PS)	–	–	–	–	–	–	–	–	–	–
PUSHW rlst	2	*3	*5	*4	(SP) ← (SP) –2n, ((SP)) ← (rlst)	–	–	–	–	–	–	–	–	–	–
POPW A	1	3	0	(c)	word (A) ← ((SP)), (SP) ← (SP) +2	–	*	–	–	–	–	–	–	–	–
POPW AH	1	3	0	(c)	word (AH) ← ((SP)), (SP) ← (SP) +2	–	–	–	–	–	–	–	–	–	–
POPW PS	1	4	0	(c)	word (PS) ← ((SP)), (SP) ← (SP) +2	–	–	*	*	*	*	*	*	*	–
POPW rlst	2	*2	*5	*4	(rlst) ← ((SP)), (SP) ← (SP) +2n	–	–	–	–	–	–	–	–	–	–
JCTX @A	1	14	0	6× (c)	Context switch instruction	–	–	*	*	*	*	*	*	*	–
AND CCR, #imm8	2	3	0	0	byte (CCR) ← (CCR) and imm8	–	–	*	*	*	*	*	*	*	–
OR CCR, #imm8	2	3	0	0	byte (CCR) ← (CCR) or imm8	–	–	*	*	*	*	*	*	*	–
MOV RP, #imm8	2	2	0	0	byte (RP) ←imm8	–	–	–	–	–	–	–	–	–	–
MOV ILM, #imm8	2	2	0	0	byte (ILM) ←imm8	–	–	–	–	–	–	–	–	–	–
MOVEA RWi, ear	2	3	1	0	word (RWi) ←ear	–	–	–	–	–	–	–	–	–	–
MOVEA RWi, eam	2+	2+ (a)	1	0	word (RWi) ←eam	–	–	–	–	–	–	–	–	–	–
MOVEA A, ear	2	1	0	0	word(A) ←ear	–	*	–	–	–	–	–	–	–	–
MOVEA A, eam	2+	1+ (a)	0	0	word (A) ←eam	–	*	–	–	–	–	–	–	–	–
ADDSP #imm8	2	3	0	0	word (SP) ← (SP) +ext (imm8)	–	–	–	–	–	–	–	–	–	–
ADDSP #imm16	3	3	0	0	word (SP) ← (SP) +imm16	–	–	–	–	–	–	–	–	–	–
MOV A, brgl	2	*1	0	0	byte (A) ← (brgl)	Z	*	–	–	–	*	*	–	–	–
MOV brg2, A	2	1	0	0	byte (brg2) ← (A)	–	–	–	–	–	*	*	–	–	–
NOP	1	1	0	0	No operation	–	–	–	–	–	–	–	–	–	–
ADB	1	1	0	0	Prefix code for accessing AD space	–	–	–	–	–	–	–	–	–	–
DTB	1	1	0	0	Prefix code for accessing DT space	–	–	–	–	–	–	–	–	–	–
PCB	1	1	0	0	Prefix code for accessing PC space	–	–	–	–	–	–	–	–	–	–
SPB	1	1	0	0	Prefix code for accessing SP space	–	–	–	–	–	–	–	–	–	–
NCC	1	1	0	0	Prefix code for no flag change	–	–	–	–	–	–	–	–	–	–
CMR	1	1	0	0	Prefix code for common register bank	–	–	–	–	–	–	–	–	–	–

*1: PCB, ADB, SSB, USB, and SPB : 1 state
DTB, DPR : 2 states
*2: 7 + 3 × (pop count) + 2 × (last register number to be popped), 7 when rlst = 0 (no transfer register)
*3: 29 + (push count) – 3 × (last register number to be pushed), 8 when rlst = 0 (no transfer register)
*4: Pop count × (c), or push count × (c)
*5: Pop count or push count.

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

Table 21 Bit Manipulation Instructions [21 Instructions]

Mnemonic		#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVB	A, dir:bp	3	5	0	(b)	byte (A) ← (dir:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB	A, addr16:bp	4	5	0	(b)	byte (A) ← (addr16:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB	A, io:bp	3	4	0	(b)	byte (A) ← (io:bp) b	Z	*	–	–	–	*	*	–	–	–
MOVB	dir:bp, A	3	7	0	2× (b)	bit (dir:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB	addr16:bp, A	4	7	0	2× (b)	bit (addr16:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
MOVB	io:bp, A	3	6	0	2× (b)	bit (io:bp) b ← (A)	–	–	–	–	–	*	*	–	–	*
SETB	dir:bp	3	7	0	2× (b)	bit (dir:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB	addr16:bp	4	7	0	2× (b)	bit (addr16:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
SETB	io:bp	3	7	0	2× (b)	bit (io:bp) b ← 1	–	–	–	–	–	–	–	–	–	*
CLRB	dir:bp	3	7	0	2× (b)	bit (dir:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB	addr16:bp	4	7	0	2× (b)	bit (addr16:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
CLRB	io:bp	3	7	0	2× (b)	bit (io:bp) b ← 0	–	–	–	–	–	–	–	–	–	*
BBC	dir:bp, rel	4	*1	0	(b)	Branch when (dir:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBC	addr16:bp, rel	5	*1	0	(b)	Branch when (addr16:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBC	io:bp, rel	4	*2	0	(b)	Branch when (io:bp) b = 0	–	–	–	–	–	–	*	–	–	–
BBS	dir:bp, rel	4	*1	0	(b)	Branch when (dir:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBS	addr16:bp, rel	5	*1	0	(b)	Branch when (addr16:bp) b = 1	–	–	–	–	–	–	*	–	–	–
BBS	io:bp, rel	4	*2	0	(b)	Branch when (io:bp) b = 1	–	–	–	–	–	–	*	–	–	–
SBBS	addr16:bp, rel	5	*3	0	2× (b)	Branch when (addr16:bp) b = 1, bit = 1	–	–	–	–	–	–	*	–	–	*
WBTS	io:bp	3	*4	0	*5	Wait until (io:bp) b = 1	–	–	–	–	–	–	–	–	–	–
WBTC	io:bp	3	*4	0	*5	Wait until (io:bp) b = 0	–	–	–	–	–	–	–	–	–	–

*1: 8 when branching, 7 when not branching
*2: 7 when branching, 6 when not branching
*3: 10 when condition is satisfied, 9 when not satisfied
*4: Undefined count
*5: Until condition is satisfied

Note: For an explanation of “(a)” to “(d)”, refer to Table 4, “Number of Execution Cycles for Each Type of Addressing,” and Table 5, “Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles.”

Table 22 Accumulator Manipulation Instructions (Byte/Word) [6 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
SWAP	1	3	0	0	byte (A) 0 to 7 ↔ (A) 8 to 15	–	–	–	–	–	–	–	–	–	–
SWAPW/XCHW AL, AH	1	2	0	0	word (AH) ↔ (AL)	–	*	–	–	–	–	–	–	–	–
EXT	1	1	0	0	byte sign extension	X	–	–	–	–	*	*	–	–	–
EXTW	1	2	0	0	word sign extension	–	X	–	–	–	*	*	–	–	–
ZEXT	1	1	0	0	byte zero extension	Z	–	–	–	–	R	*	–	–	–
ZEXTW	1	1	0	0	word zero extension	–	Z	–	–	–	R	*	–	–	–

Table 23 String Instructions [10 Instructions]

Mnemonic	#	~	RG	B	Operation	LH	AH	I	S	T	N	Z	V	C	RMW
MOVS/MOVSI	2	*2	*5	*3	Byte transfer @AH+ ← @AL+, counter = RW0	–	–	–	–	–	–	–	–	–	–
MOVSD	2	*2	*5	*3	Byte transfer @AH– ← @AL–, counter = RW0	–	–	–	–	–	–	–	–	–	–
SCEQ/SCEQI	2	*1	*5	*4	Byte retrieval (@AH+) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
SCEQD	2	*1	*5	*4	Byte retrieval (@AH–) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
FISL/FILSI	2	6m +6	*5	*3	Byte filling @AH+ ← AL, counter = RW0	–	–	–	–	–	*	*	–	–	–
MOVSW/MOVSWI	2	*2	*8	*6	Word transfer @AH+ ← @AL+, counter = RW0	–	–	–	–	–	–	–	–	–	–
MOVSWD	2	*2	*8	*6	Word transfer @AH– ← @AL–, counter = RW0	–	–	–	–	–	–	–	–	–	–
SCWEQ/SCWEQI	2	*1	*8	*7	Word retrieval (@AH+) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
SCWEQD	2	*1	*8	*7	Word retrieval (@AH–) – AL, counter = RW0	–	–	–	–	–	*	*	*	*	–
FILSW/FILSWI	2	6m +6	*8	*6	Word filling @AH+ ← AL, counter = RW0	–	–	–	–	–	*	*	–	–	–

m: RW0 value (counter value)
n: Loop count

*1: 5 when RW0 is 0, 4 + 7 × (RW0) for count out, and 7 × n + 5 when match occurs
*2: 5 when RW0 is 0, 4 + 8 × (RW0) in any other case
*3: (b) × (RW0) + (b) × (RW0) when accessing different areas for the source and destination, calculate (b) separately for each.
*4: (b) × n
*5: 2 × (RW0)
*6: (c) × (RW0) + (c) × (RW0) when accessing different areas for the source and destination, calculate (c) separately for each.
*7: (c) × n
*8: 2 × (RW0)

Note: For an explanation of "(a)" to "(d)", refer to Table 4, "Number of Execution Cycles for Each Type of Addressing," and Table 5, "Correction Values for Number of Cycles Used to Calculate Number of Actual Cycles."

MB90670/675 Series

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Part number	Package	Remarks
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MB90676PFV MB90677PFV MB90678PFV MB90T678PFV MB90P678PFV	100-pin Plastic LQFP (FPT-100P-M05)	
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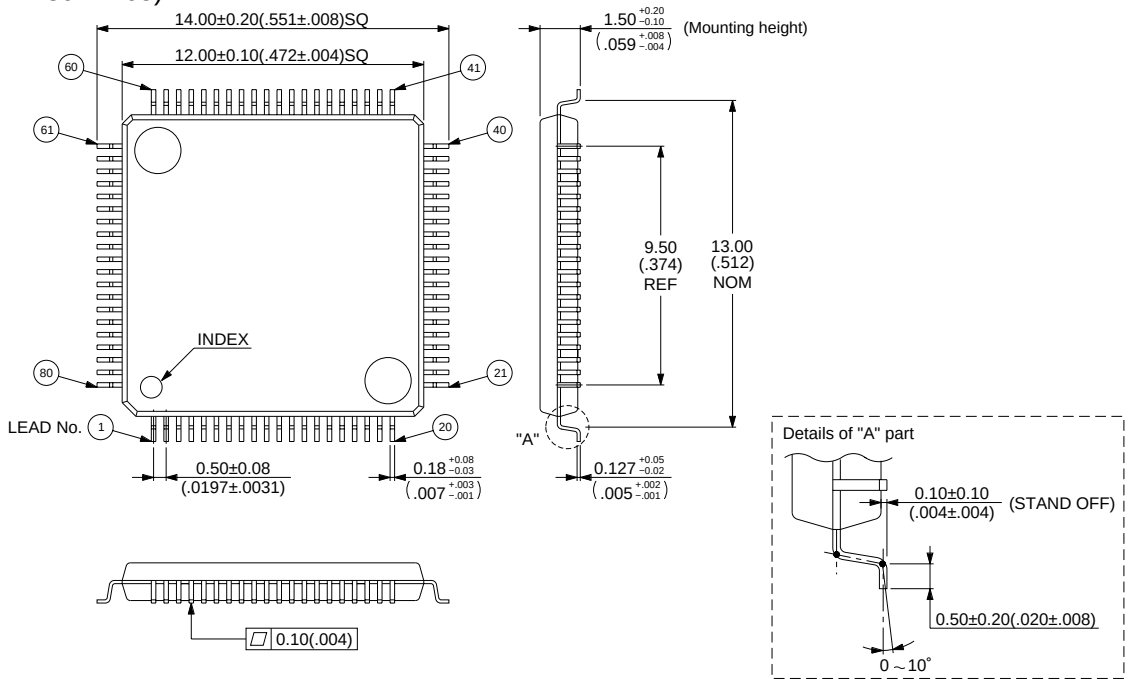
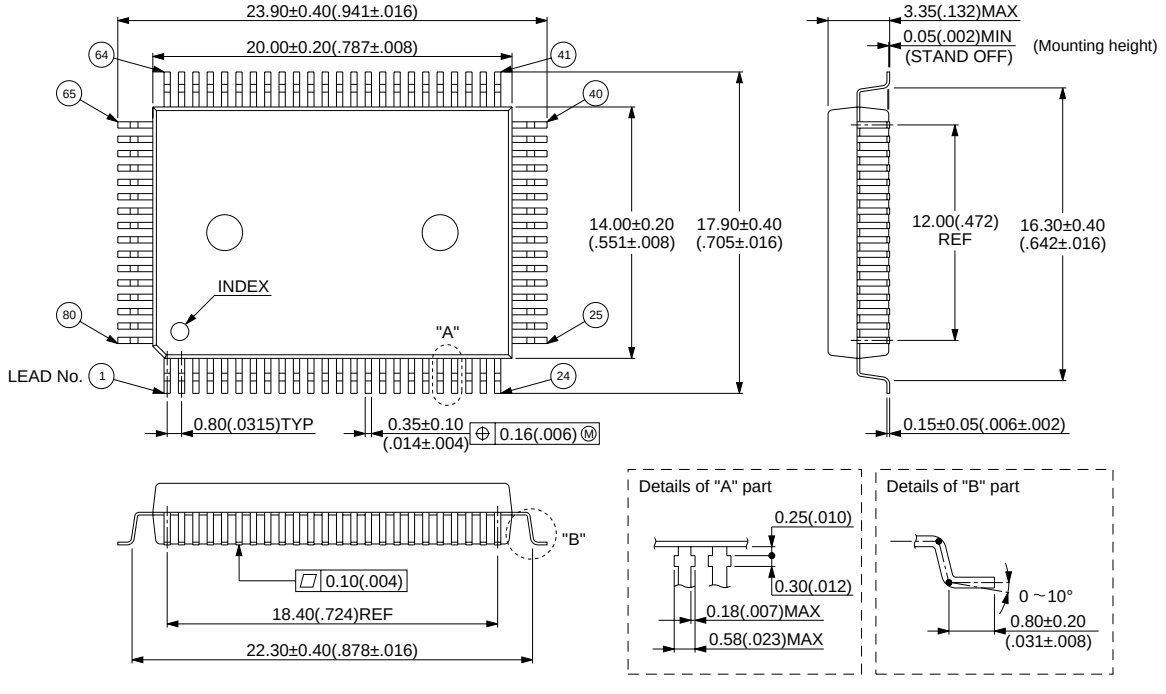
■ PACKAGE DIMENSIONS

80-pin Plastic LQFP
(FPT-80P-M05)



Dimensions in mm (inches)

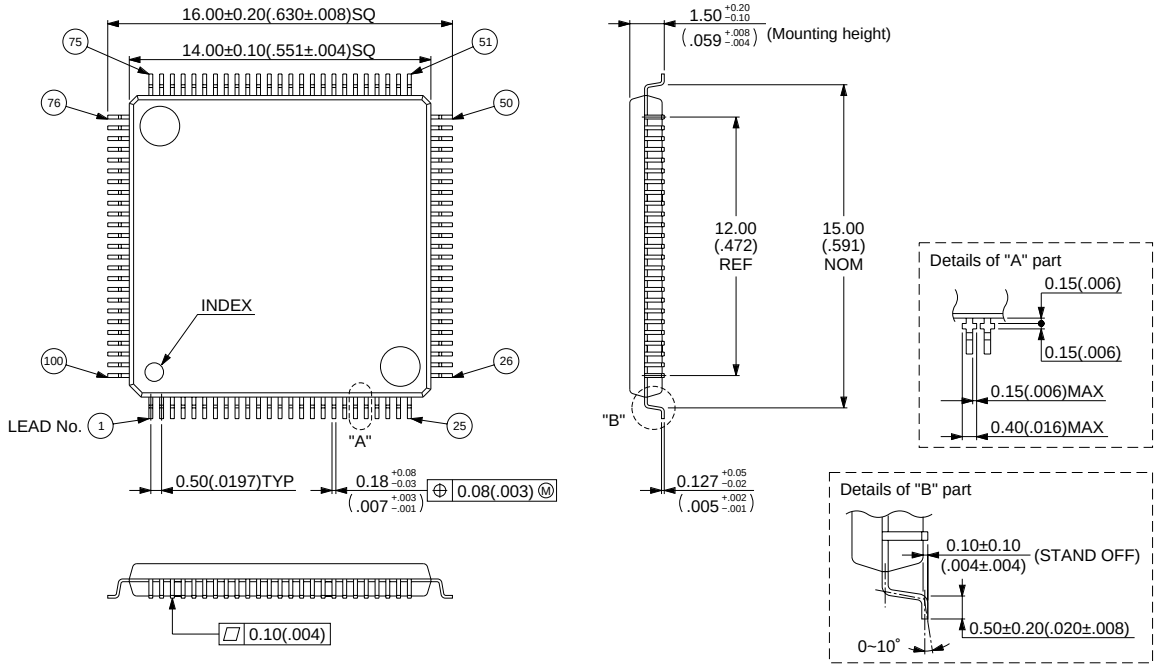
80-pin Plastic QFP
(FPT-80P-M06)



Dimensions in mm (inches)

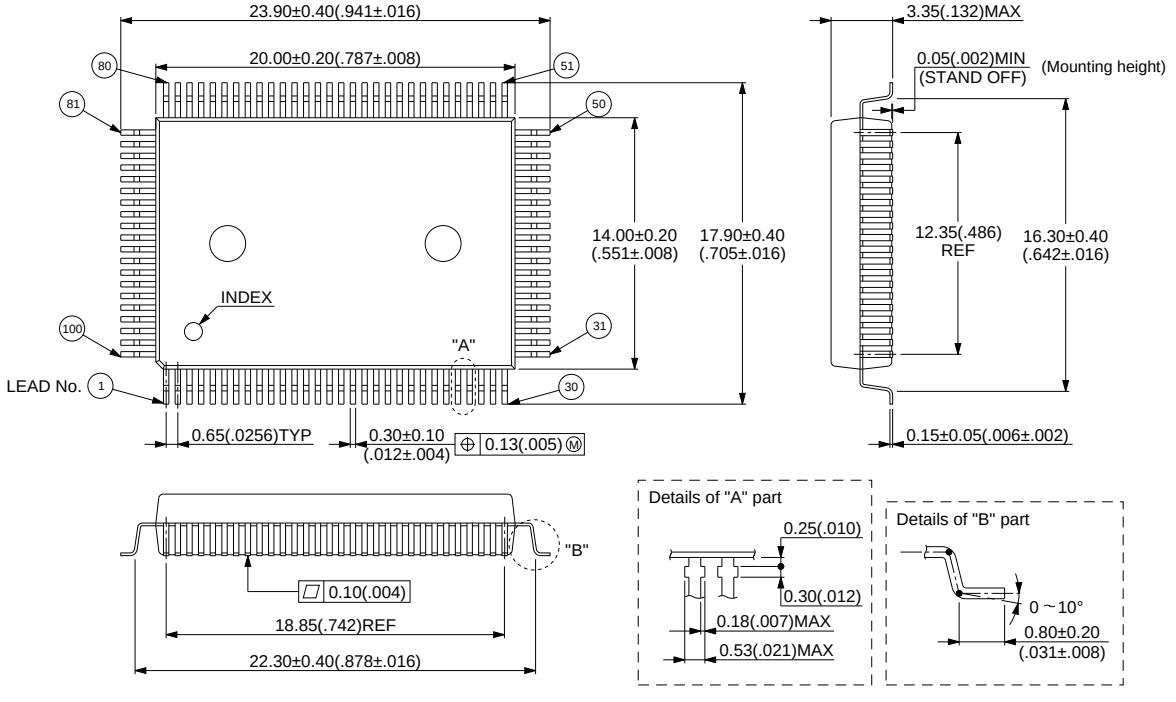
MB90670/675 Series

100-pin Plastic LQFP
(FPT-100P-M05)



Dimensions in mm (inches)

100-pin Plastic QFP
(FPT-100P-M06)



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FUJITSU LIMITED

For further information please contact:

Japan
FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-88, Japan
Tel: (044) 754-3763
Fax: (044) 754-3329

http://www.fujitsu.co.jp/

North and South America
FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, U.S.A.
Tel: (408) 922-9000
Fax: (408) 922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: (800) 866-8608
Fax: (408) 922-9179

http://www.fujitsumicro.com/

Europe
FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
D-63303 Dreieich-Buchschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

http://www.fujitsu-ede.com/

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE LTD
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

http://www.fmap.com.sg/

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